Report of visit to Bologna, summer 2003

Peter Stallinga, August 2003

on the picture from left to right: Carlo Taliani, Mauro Murgia, Rafaella Capelli, Peter Stallinga, Roberto Zamboni, Clara Santato, Michele Muccini, V.A.L. Roy, Fabio Cicoira

The FlexiFET program

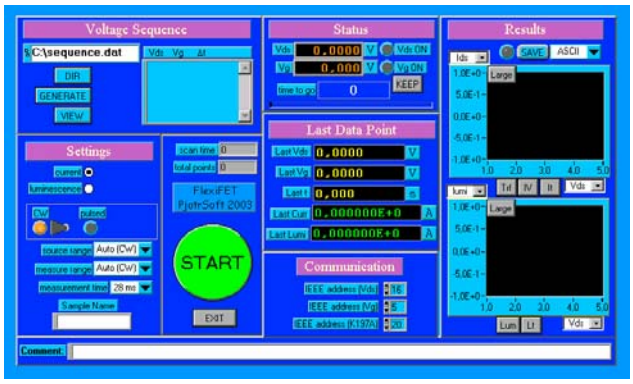
After some days of stiff programming there is the new PjotrSoft FET measurement program, FlexiFET™, which can also make transients and is, in principle, more flexible to operate. The user supplies a file with the data points to be measured. The program then executes this sequence file. Alternatively, the program can generate a sequence automatically. In this way preprogrammed curves can be made:

- (Multiple) IV curves
- (Multiple) transfer curves

New features are

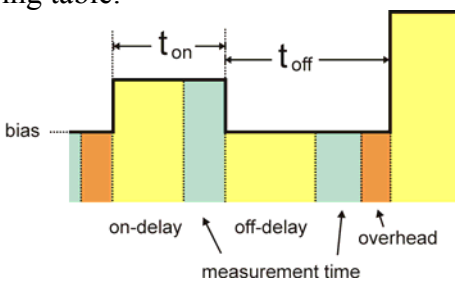
- Voltaic transients; define two voltages and specify how long the program should measure at those two voltages.
- Locus curves (*Vg* fixed to *Vds*)
- Hysteresis

If the need arises for other sequences, the user can edit a sequence file and load that into the program.



(Final version: 1 August 2003)

Measurements in pulse mode: The same restrictions apply to FlexiFET as applied to the previous versions (BolognaFET and OptoFET): Both the "off time", as specified as the interval time in the sequence file, and the "on time", as specified as the pulse width, should be long enough to accommodate both the measurement time as well as the default delay, see Figure below (overhead is communication between device and computer). The default delay depends on the measurement range according to the following table:



Measure Time
1 ms
5 ms
28 ms[1,2]

I-Measure Range[3]	Default Delay
1 nA	360 ms
10 nA	75 ms
100 nA	20 ms
1 µA	5 ms
10 µA	2 ms
100 µA	0
1 mA	0
10 mA	0
100 mA	0

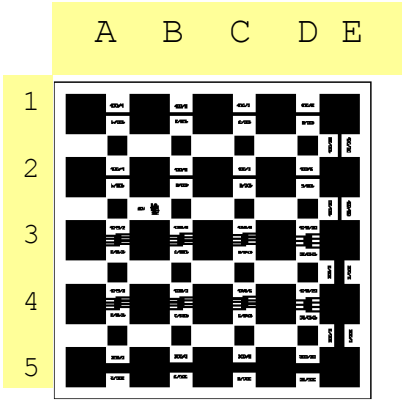
1: 50 Hz power supply, 2: 1 ms longer than Keithley manual, 3: Autorange not possible in pulsed mode

In more detail, this is what the program does in a sweep:

1. Set the Agilent 6634B voltage (normally the gate)
2. Set the Keithley 236 voltage (normally the drain). Give a trigger.
3. Wait the programmed delay (the time set in the sequence of data points). This is a delay in the computer.
4. Receive the instrument readings. In case of CW this means giving a second trigger to really start measuring. In case of pulsed mode triggering is not needed and it only means receiving the value. If the programmed delay was positive, the measurement is added to the data record (and later saved to file). Case negative, the received data are ignored.
5. Go to the next point in the sequence.

Leuven FETs

The devices made from tetracene deposited on top of the Leuven substrates show huge currents that cannot be attributed to the FETs. They are either due to charging of the oxide capacitor (displacement current) or direct leakage through the oxide or around the edges of the substrates.

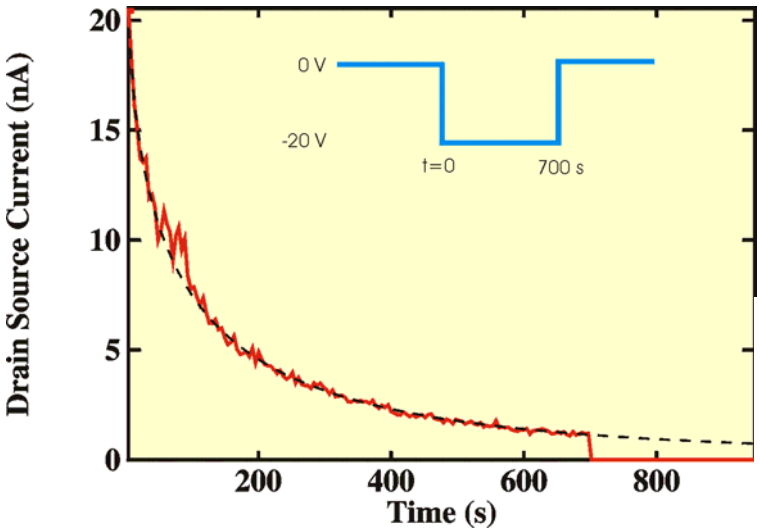


		A	B	C	D	E
1	*W/L*	100/1	100/2	100/3	100/5	100/20
2	*W/L*	100/1	100/2	100/3	100/5	100/20
3	*W/L*	1019/2	1029/3	1048/5	1010/20	300/2
4	*W/L*	1019/2	1029/3	1048/5	1010/20	300/3
5	*W/L*	300/2	300/3	300/5	300/20	

values in μm

Figure and Table: Devices on a Leuven plate. Oxide thickness: 100 nm.

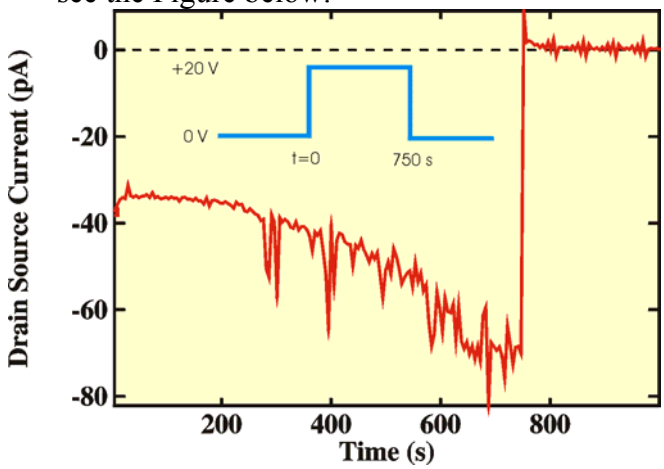
Distortions in the current curves



Transient.
Vg = 0 to -20 to 0 V, with Vd and Vs at 0 V. Sample: 1048-5-2 in integrating sphere (vacuum). 29.07.2003

In a transient of the gate voltage (0 to –20 V, with V_d and V_s at 0 V) a large, decaying current is observed. Some observations of this current

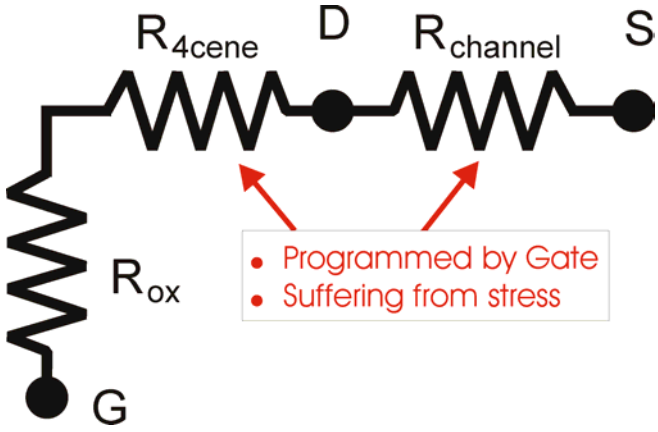
1. The current is much larger than can be expected from a displacement current. When integrated, the amount of charge put in the device, Q, is much more than the expected $Q = \Delta V\, A\, C_{ox}$: $\Delta V = 20$V, $A = 1$ cm^2, $C_{ox} = \varepsilon_0\varepsilon_r/d_{ox} = (8.85\text{x}10^{-12}$ F/m) x (3.9) / ($100\text{x}10^{-9}$ m) = 345 μF/m^2. Q = 20 x $1\text{x}10^{-4}$ x $345\text{x}10^{-6}$ = $6.91\text{x}10^{-7}$ C.
2. The current cannot be displacement current because when the voltage is removed, the charge doesn't come out. See the above figure. After 700 seconds the gate voltage was switched from –20 V to 0 V and the current immediately disappears, without any transient (displacement) effects.
3. The current follows the square-root-of-time behavior:
$$I_{ds} = I_0 \exp(-(t/\tau)^{0.5}) + I_{off}$$
The dashed line in the figure above is a fit with the parameters: $I_0 = 25.052$ nA, $\tau = 66.096$ s, $I_{off} = 0.171$ nA.
4. Repeating the measurement after 20 minutes wait gives very similar result (slight decrease in currents; starts at 15 instead of 20 nA).
5. Note: the source current is not measured. Not all the current is therefore measured. I assume that 50% of the current comes from the drain and 50% from the source. All the plots have to be scaled by 2.
6. For putting positive voltages on the gate the transients look entirely different, see the Figure below:



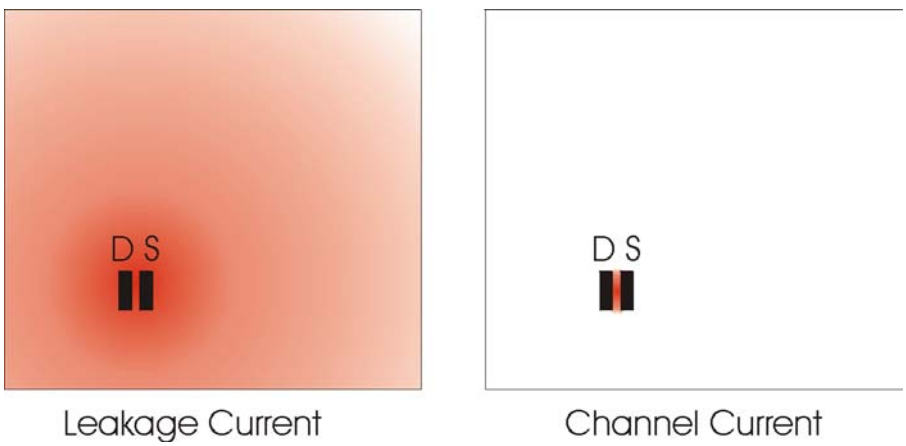
*Transient on the same sample with **positive** gate voltage. Note the different scale.*

The model:

- These are **not displacement** currents in the sense that a capacitor is charged.
- Leakage from drain to gate has to go through the tetracene layer.
- This can only occur if there are mobile carriers there. When the "channel" is open. ("Channel" in quotes, because it is not the channel between source and drain, but rather a sheet of charge in the entire tetracene film).
- When mobile charges are available, they will be trapped, thus the channel slowly **closes**. Hence a slowly decaying current in the transient (negative Vg).
- The shape of the transient (exponent of square-root of time) sheds light on the states responsible for trapping the holes. Probably trap states with a Gaussian distribution in energy.
- For negative positive gate voltages, the channel does not open. We see a slowly increasing tiny current, which might be the result of detrapping of holes in some way.
- The maximum real leakage **through** the gate can be calculated. In the worst-case scenario the resistivity of SiO_2 is 10^{14} Ωcm. With the oxide layer dimensions (1 cm^2 and 100 nm) this means a resistance of 10^7 Ω and a current at 20 V of 2 μA. In principle enough to sustain the currents of the figures above. In the best-case scenario this would be 100 times lower 20 nA, just enough to explain the currents. (Resistivity values taken from Sze).



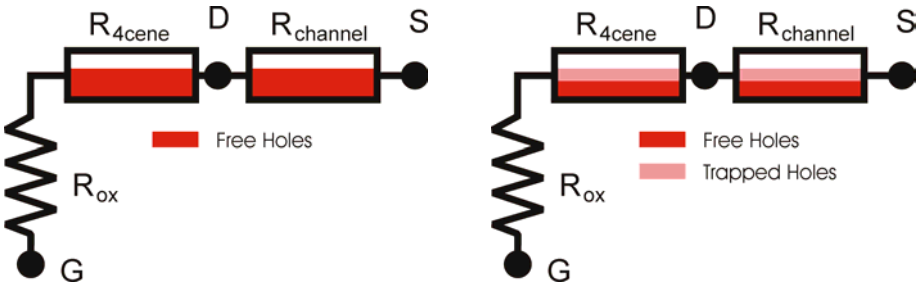
The figure above shows the proposed model. The resistances of the channel $R_{channel}$ and the rest of the tetracene R_{4cene} are programmed by the gate and suffer from stressing (trapping of holes). Relatively, the oxide resistance is less than the other resistances. Moreover, $R_{channel} \approx R_{4cene}$, but varies slightly from device to device.



The conclusion:

- The leakage is a normal leakage current through the oxide, which decays over time because the resistance of the tetracene layer is increasing with time, see below.
- There is no current "around the edge". There is no use in masking the edge!

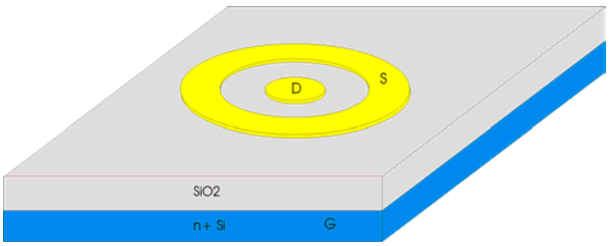
Stressing model to explain the transients



Left: When the gate is switched on, free holes are created in the channel *and* in the rest of the plate. The leakage current is of the same magnitude as the channel current. **Right**: After a while some of the free holes have become trapped. Whilst still contributing to the charge ($Q = CV$), they no longer contribute to the current and hence the current drops.

Circumventing the leakage currents

- Circular FETs. In this way, the path from drain to gate is limited, see figure below.

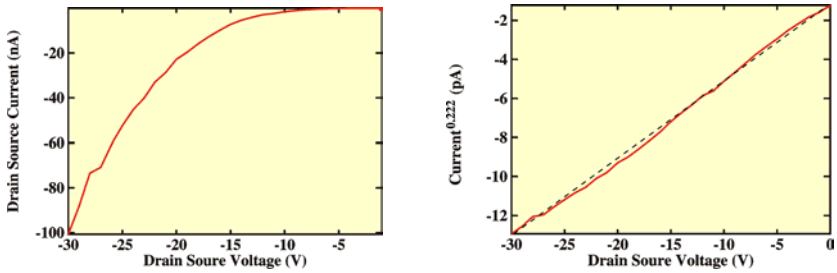


In this way the leakage current is reduced. The active area for this is now only the area within the source electrode. On the other hand, the channel current is increased because looking from the drain electrode the source is seen in all directions.

Poor man's alternative:

- Scratch or mask the sample to isolate a single device.
- Connect the pads on the side of the device to the source to make some kind of guard ring around a device.
- Measuring locus curves (with $Vds = Vg$)

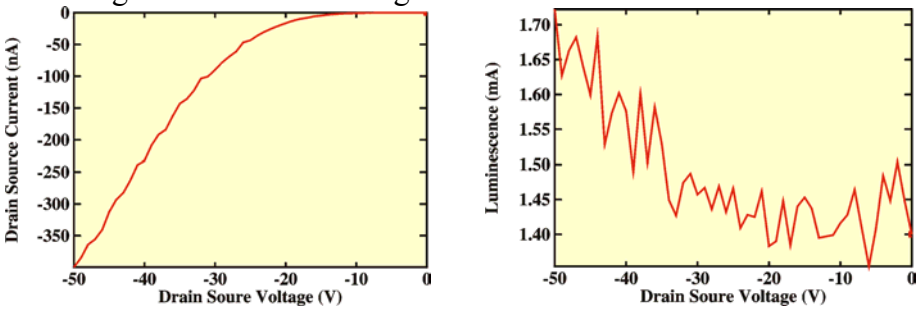
Locus Curve



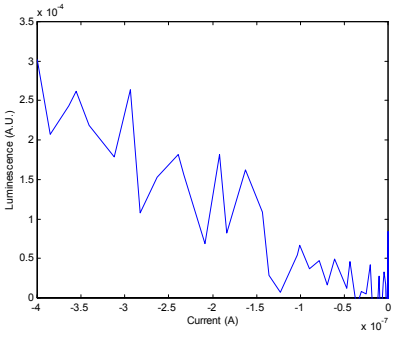
Locust curves for the same device as above. (Vg=Vds). On the right plotted as the 4.5th root of the current. 30.07.2003

As can be seen, in the locust curves, as expected, we don't have any leakage curves anymore. The curves are not yet standard FET curves yet, though. The locust curves should be quadratic ($I \sim V^2$), but instead they follow $I \sim V^{4..5}$, as can be seen in the Figure above.

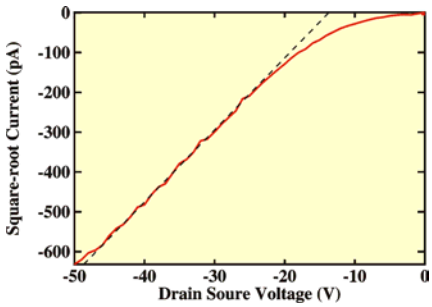
For higher voltages and also measuring the luminescence:



Locus curves (Vg=Vds) of current (left) and luminescence (right). Sample the same as above. (Files: `loclumi.m`, `loclum1.m`*)*



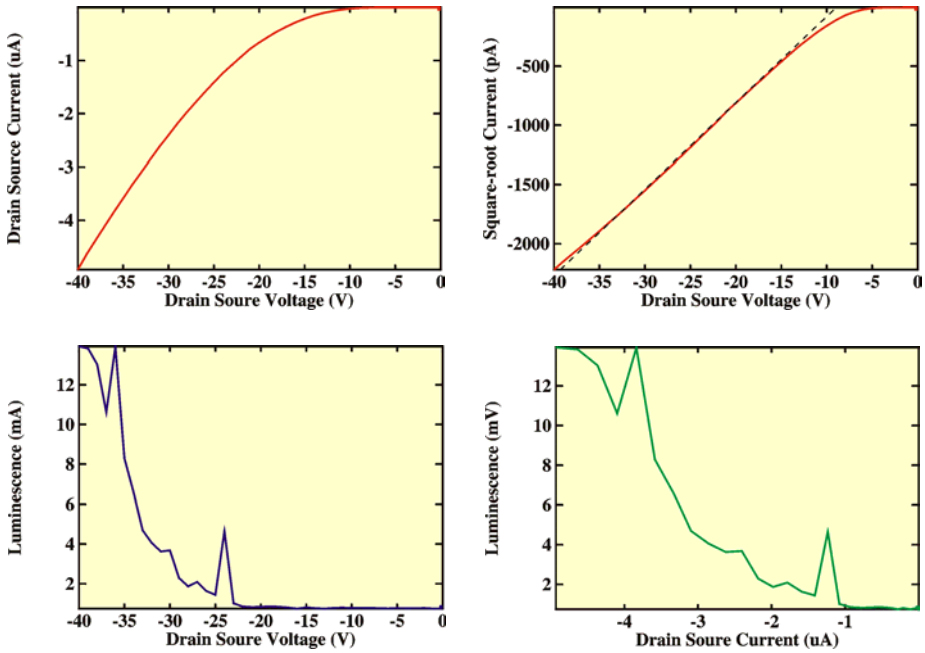
Plot of luminescence versus current. Linear dependence. (An offset of 1.43mV was subtracted from the luminescence values.



Using the saturation model for the locus curves yields a mobility of 9.3×10^{-5} cm^2/Vs, see dashed line.

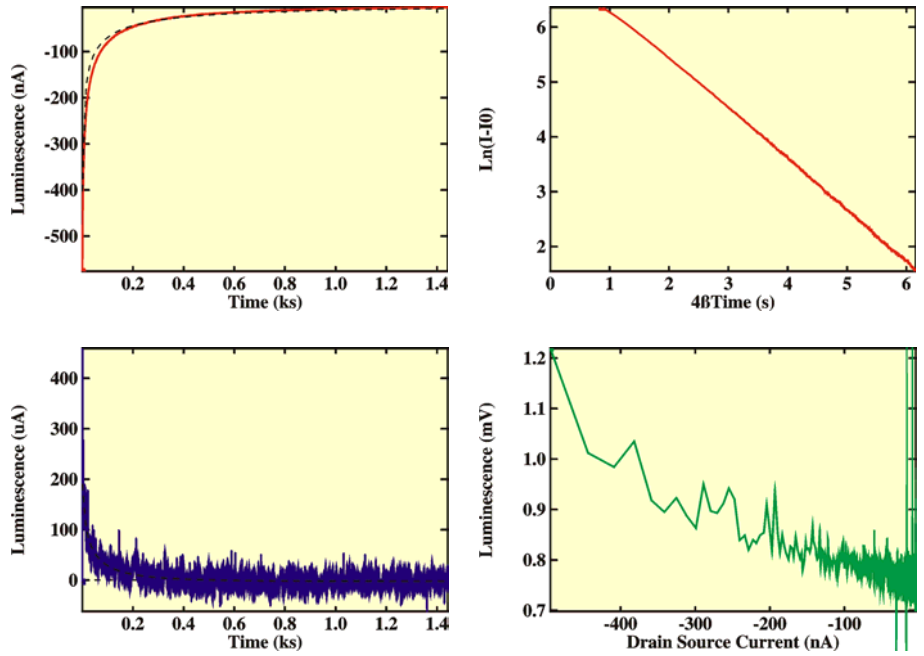
Fresh samples

New samples grown on 1 August. measured directly in the integrating sphere. Device D4 (W = 1010 μm, L = 20 μm):

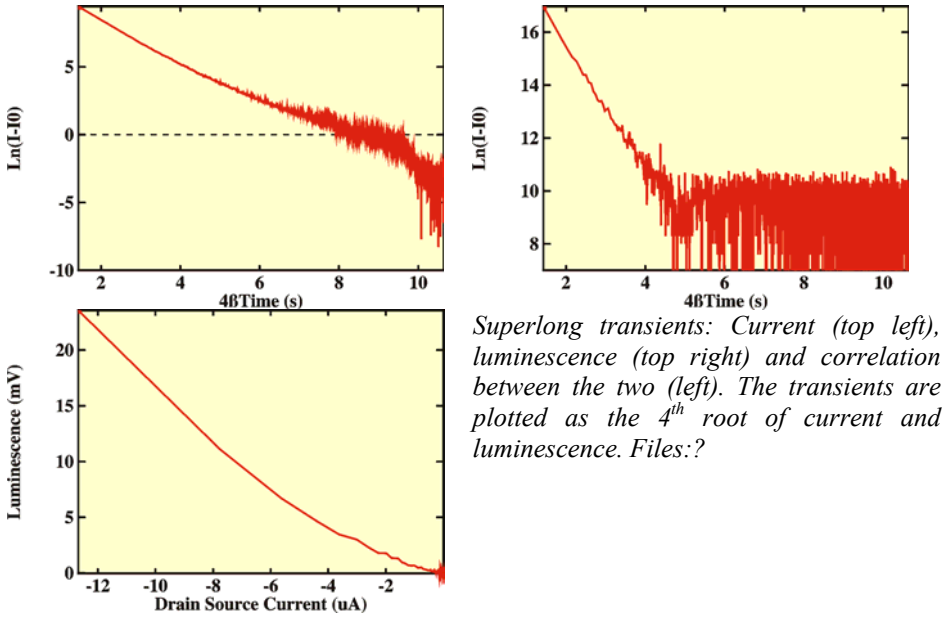


From left to right locus curves: IV, Square-root IV, LV, correlation L-Ids. From second plot: mobility is 6.31 10^{-3} cm^2/Vs. Files:

Transients

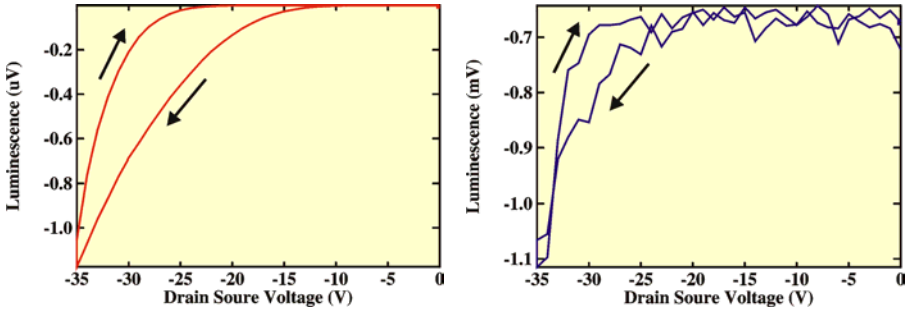


From left to right transients: IV, Fourth-root IV, LV (with square-root fit), correlation L-Ids. Files: TRIL_C3 of 07/08/2003. Again, a linear correlation between the current and the luminescence is observed.

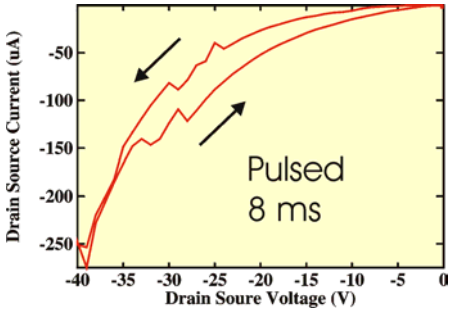


Superlong transients: Current (top left), luminescence (top right) and correlation between the two (left). The transients are plotted as the 4th root of current and luminescence. Files:?

Hysteresis



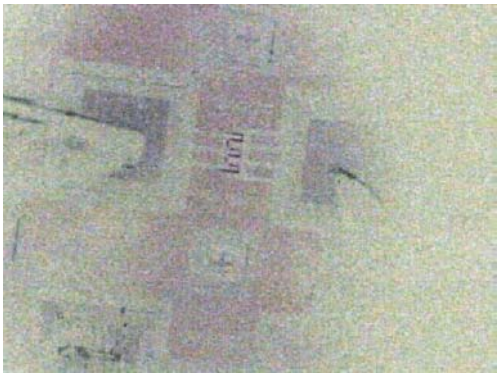
The picture on the left shows a current locus curve, with Vg=Vds from 0 to –40 V back to 0. The right picture shows the accompanying luminescence (file: `1029-3pmt1100n2.m` [`hyster.m`] taken on 21-08-2003). The hysteresis shows that we have stressing going on during (on the time scale of) the measurement. This is better studied with transients as described above.



The Figure on the left shows the hysteresis in pulsed mode (8 ms pulses). In this case the current in the returning curve is higher. There is no luminescence signal when using pulse mode, because by the time the data is read from the Keithley DMM, the pulse has finished.

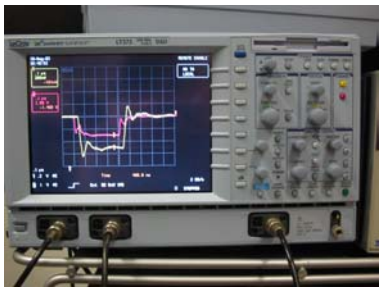
Data taken on 10 August. File: `Hyster current&lumi Pulse 0to-40B4.m`

Luminescence visible by eye



Left: Electro-luminescence curves overlapped with device layout. On the right the images is inverted to enhance visibility

ScopeFET setup

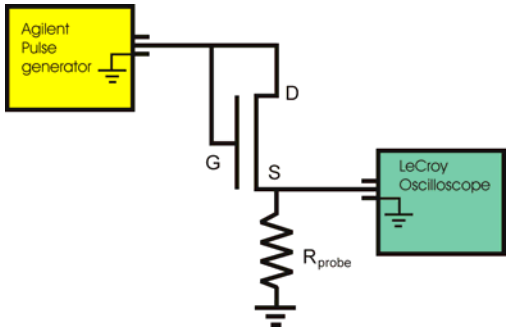


The idea of ScopeFET is to apply super-short pulses (Agilent) to the transistors and measure the current using an ultra-fast oscilloscope (LeCroy). The picture on the left shows the result of the first test run of the ScopeFET setup. It shows two traces. The red one is the pulse as given to the drain (–2 V, 400 ns). The yellow trace is the voltage at the source, which is in this case about –0.5 V. The probe resistance used in this case was 50 Ω, so this translates to a drain-source current of –10 mA at a drain-source voltage of –1.5 V. The picture below shows the setup used to acquire these results. This is setup "A". The probe resistance was located in the dangling gray metal box. The output terminal at the bottom of the box was short-circuited to ground (the box itself). The output of the pulse generator was connected to channel 2 of the oscilloscope (not shown on the picture on the left). The drain was connected to channel 1, as shown.

TABLE: EQUIPMENT USED IN THE EXPERIMENT

Agilent 8114A	Pulse generator, 20 ns to x s, +/- 100 V, 2 A
LeCroy LT372	Oscilloscope, 2 channels, 4 Gs/s
HP 6002A	Programmable Power supply
Agilent 82357A	IEEE USB interface
Visual Basic 6.0	Programming environment

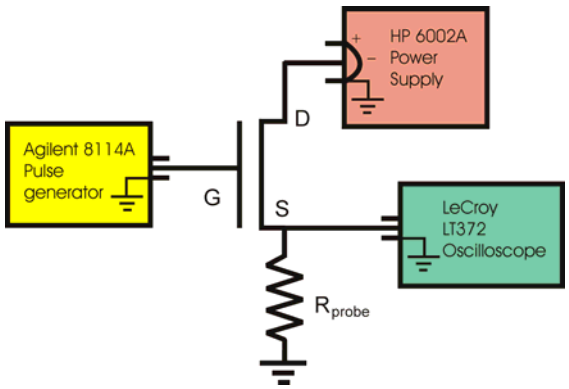
A



Description: Locus full pulse. Both drain and gate pulsed
Advantage: Easiest set up.
Disadvantage: Only locus curves. Also leakage current measured.

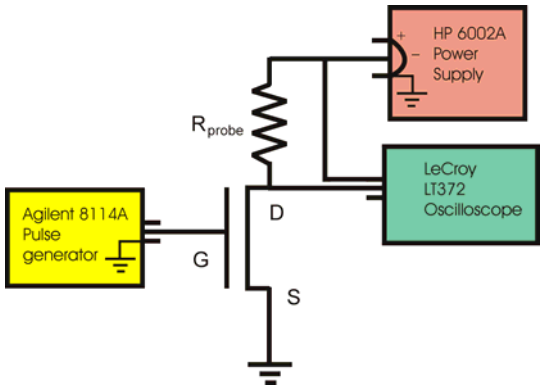
Alternative setup

B



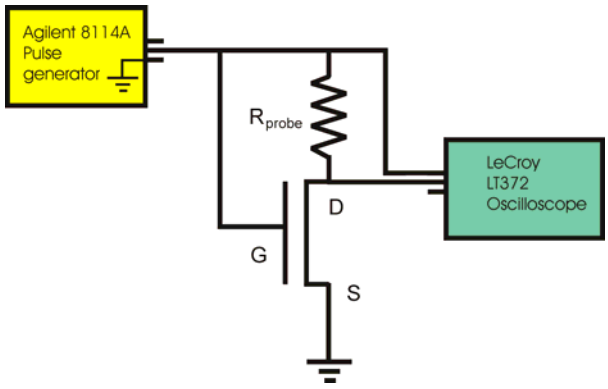
Description: Gate pulsed. Drain DC and is supplied by HP 6002A power supply. Drain voltage is negative, so no stressing effects (when pulse is off, no holes are attracted to interface)
Advantage: Independent gate and drain. Only gate is pulsed.
Disadvantage: Gate - source leakage still measured.

C



Description: Probe resistance measures drain current. Oscilloscope is not grounded.
Advantage: Independent gate and drain. No leakage if *Vd* = *Vg*
Disadvantage: Gate - drain leakage still measured if *Vd* <> *Vg*.

D



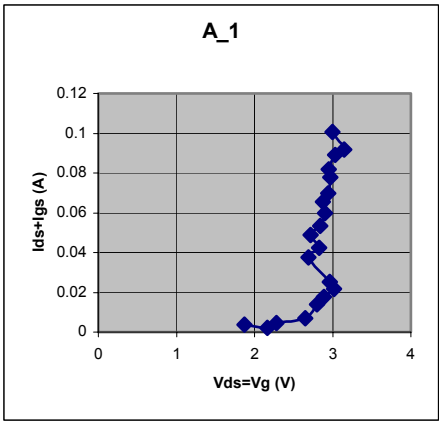
Description: Both gate and drain are pulsed. Only drain current measured. Very good for leaky devices!
Advantage: No leakage; accurate *Ids* measurement.
Disadvantage: Oscilloscope not grounded. Only locus curves.

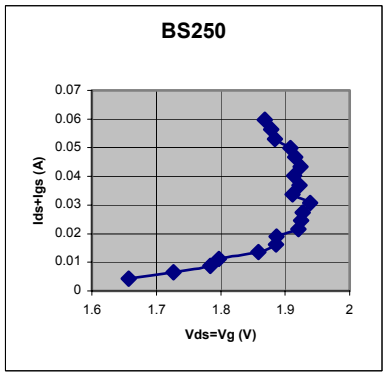
First measurement on a device (OTS treated device, kept in the glove box for the weekend). The setup used was type "A". See data in Table and Figure below. Explanation of the table:

1. The first column shows the programmed pulse height.
2. The second column shows the voltage over the probe resistance (source).
3. The third column is the as-measured pulse height, which is differing from the first column because the resistance of the load of the system (FET plus probe resistance) is low compared to the output resistance of the Agilent Pulse Generator (50 Ω). The Agilent can, in principle, correct for this ("expected load impedance", see below) but that was not done in this case (it was set to 999 kΩ).
4. The fourth column is the drain-source voltage, which is the as-measured pulse height minus the probe voltage. This is also equal to the gate-source voltage.
5. The fifth column shows the FET current (*Ids* + *Igs*), which is measured from the probe voltage divided by the probe resistance (10 Ω in this case).

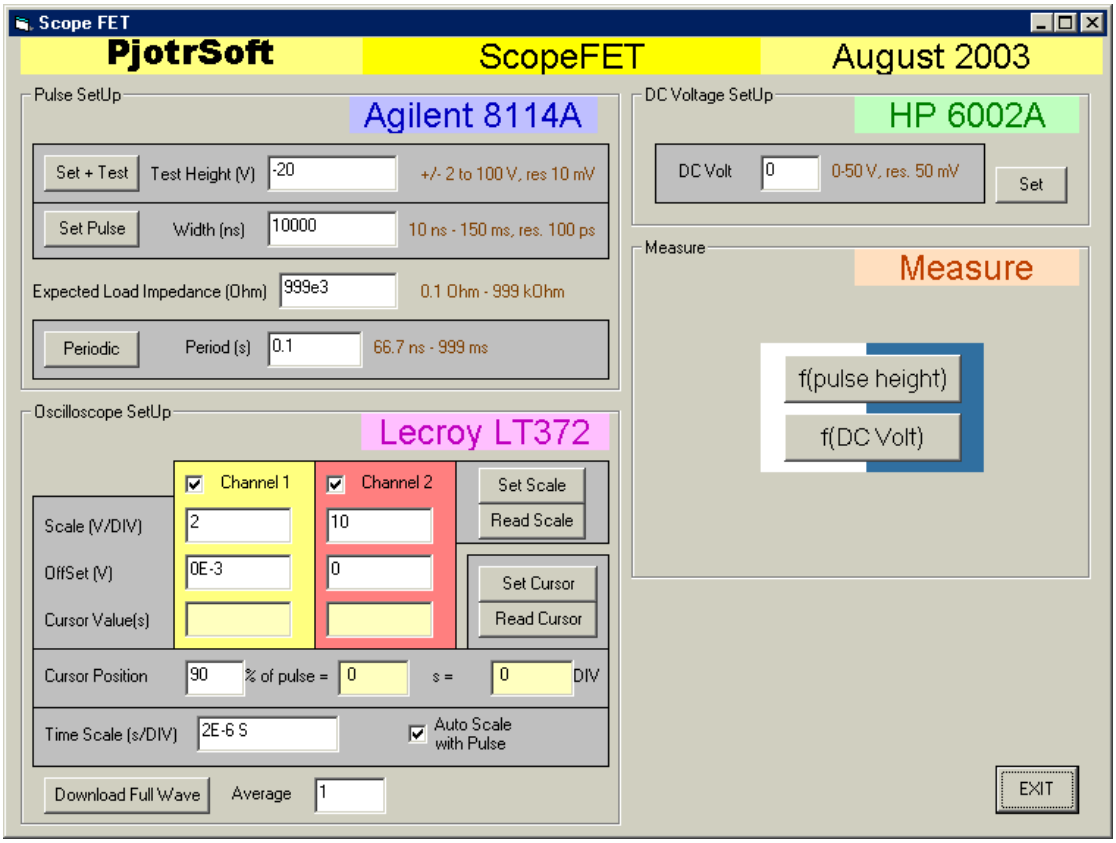
Vprog	Vprobe	Vpulse	Vds (V)	Ids (A)
2	0.0375	1.90625	1.86875	0.00375
2.4	0.021875	2.1875	2.165625	0.002188
2.8	0.046875	2.328125	2.28125	0.004688
3.2	0.06875	2.71875	2.65	0.006875
3.6	0.140625	2.9375	2.796875	0.014063
4	0.178125	3.0625	2.884375	0.017813
4.4	0.21875	3.234375	3.015625	0.021875
4.8	0.253125	3.21875	2.965625	0.025313
5.2	0.375	3.0625	2.6875	0.0375
5.6	0.425	3.25	2.825	0.0425
6	0.4875	3.203125	2.715625	0.04875
6.4	0.534375	3.375	2.840625	0.053438
6.8	0.6	3.5	2.9	0.06
7.2	0.65625	3.53125	2.875	0.065625
7.6	0.696875	3.640625	2.94375	0.069688
8	0.778125	3.75	2.971875	0.077813
8.4	0.81875	3.765625	2.946875	0.081875
8.8	0.890625	3.921875	3.03125	0.089063
9.2	0.91875	4.0625	3.14375	0.091875
9.6	1.00625	4	2.99375	0.100625

file: A_1.DAT. Absolute values.





Compared to a commercial device (BS250 of Philips). Measured with setup A, 1 µs pulse, 999 kΩ load resistance. 0 to –10 V programmed pulse height.

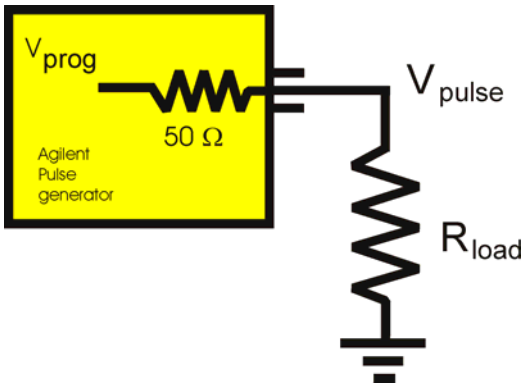


Normal mode of operation:

1. Set up the pulse and oscilloscope until you get a good signal on the screen; either change the scale on the oscilloscope or on the computer. Then make sure that the computer settings and the oscilloscope settings are equal ("Set Scale" or "Read Scale"). As a special feature, to facilitate setting up the equipment, also periodic signals can be applied.
2. Specify where you want to measure the signal by specifying the position of the cursors (not needed for full waveform measurements, see below).
3. There are now three types of measurements
    a. Full Waveform Transfer. This transfers the entire screen, as seen on the oscilloscope to the computer. This can be a lot of data (up to 100 thousands data points on a screen, resulting in up to 2 MB of data per channel). In this way, Fourier-transform spectroscopy can be done.
    b. DC scanning. The pulse height is fixed and the DC (HP Power supply is fixed). Only positive voltages can be output; if negative voltages are needed, the power supply has to be rewired. This can be used to make IV curves (set up type "C").
    c. Pulse-height scanning. The DC voltage is fixed and the pulse height is scanned. In this way transfer curves can be made (setup type "D") or full-pulse measurements can be done with setup type "A".

Expected load resistance:

The output resistance of the Agilent pulse generator is 50 Ω. When the load of the measured system (FET plus probe resistance) is low, a substantial part of the programmed voltage is lost internally, inside the Agilent. For instance, if the load



resistance is 25 Ω, and a 10 V pulse is programmed, the actual voltage coming out of the Agilent will be 3.33 V; the 50 Ω of the Agilent and the 25 Ω of the load act as a voltage divider. *Vpulse* = *Vprog***Rload*/(*Rload*+50 Ω).

The Agilent 8114A can correct for this by specifying the expected load resistance. But, **be careful with this**. If you set the load resistance too low, for instance 1 Ω, a programmed pulse of 2 V will be set as an internal 100 V pulse. If the real resistance *Rload* is now large, this 100 V will appear on your device, possibly burning it.