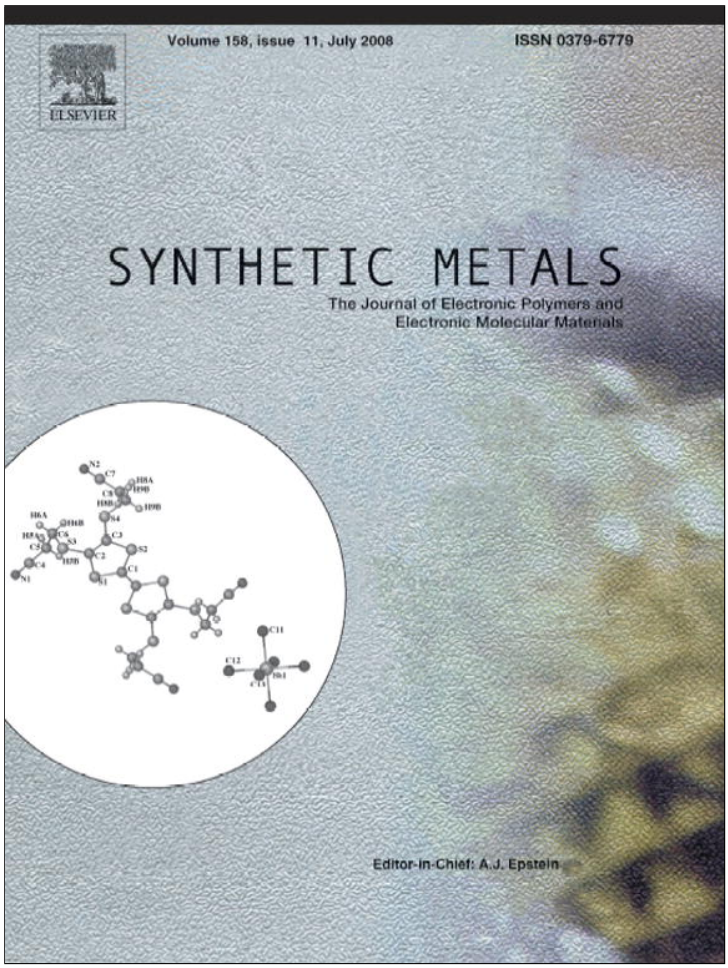

Synthetic Metals 158 (2008) 473–478

Contents lists available at ScienceDirect

Synthetic Metals

journal homepage: www.elsevier.com/locate/synmet

Modeling electrical characteristics of thin-film field-effect transistors III. Normally-on devices

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ARTICLE INFO

Article history:
Received 14 March 2007
Accepted 18 March 2008
Available online 1 May 2008

PACS:
85.30.De
85.30.Tv

Keywords:
Thin-film field-effect transistors
Organic semiconductors
Two-dimensional electronics
Metal–insulator–metal transistor

ABSTRACT

The thin-film field-effect-transistor model recently developed is applied to devices based on materials that already show current even without a bias present at the gate resulting in so-called normally-on transistors. These fall in three categories: (i) narrow-band-gap semiconductors, where the thermal energy is sufficient to excite carriers across the band-gap, here analyzed for unipolar and ambipolar materials, (ii) doped semiconductors, and (iii) metals. It is shown what the impact is on the IV and transfer curves.

1. Introduction

The thin-film transistor (TFT) structure is ever gaining in popularity because of its ease of production and its flexibility in design. In principle, any semiconducting material can be used as the active layer and it does not even have to have a perfect lattice match with the underlying substrate material. Moreover, because the film is thin and deposited by a variety of techniques, they can be made in all technological sectors, from high performance to very cheap. In contrast, a metal-oxide-semiconductor field-effect transistor is normally made from same material and the choice of devices is therefore limited with the main innovation lying in the device geometry design. TFTs thus find especially many applications in organic devices where flexibility is a must, although amorphous silicon TFTs still outnumber the organic counterparts.

In a recent publication, we successfully modeled the electrical characteristics of thin-film transistors (TFTs) based on organic and inorganic semiconductors [1], thus substituting the MOS-FET model conventionally used also for TFTs for lack of alternatives. The main difference between the MOS-FET model and the TFT model is that the latter treats the active layer more adequately as two-dimensional whereas in the MOS-FET model it is considered three-dimensional. The TFT model was developed with intrinsic, wide-band-gap materials in mind, where the room-temperature, zero-bias carrier density was negligible. The model covered both unipolar and ambipolar materials, the difference being high mobility for one type or for both types of carrier, holes and electrons. However, the range of materials is far bigger than these wide-band-gap pure materials. Especially in organics, with their sheer infinite number of possible configurations, the materials can behave from metallic up to insulating with band gaps ranging from very small to zero to very large and can be ranging from crystalline to amorphous and from ultra-pure to highly contaminated. It is interesting to determine what happens if the limitation of zero charge at zero-bias is removed. In a second work, we modeled the effects of traps (localized electronic states that can capture the free charge carrier) [2], which explains the temperature and bias-dependent mobility (including the Meyer–Neldel rule) often observed in low-mobility materials. However, we still considered the carrier density to be zero in the absence of bias. In the current work we model TFTs based on materials with substantial amounts of free charge at zero-bias, which can be divided into three classes: narrow-band-gap semiconductors, doped semiconductors, and metals.

2. Background

Before continuing, it is useful to do a small revision of the basic ingredients of the thin-film transistor model. Fig. 1 shows a cross-section of a TFT and the names for the variables used in this work. The device consists essentially of three layers: a gate, an insulator

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doi:10.1016/j.synthmet.2008.03.011

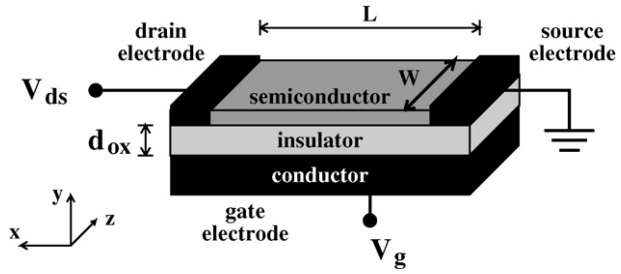

Fig. 1. Cross-section of a thin-film FET showing the nomenclature used in the current work.

and an active layer. The gate layer should be made of a conductive material (metal or semiconductor) that is used to induce charge in the active layer. The insulator separates the gate from the active layer and has only the function of preventing charge flowing from the active layer to the gate. The active layer, as demonstrated in the previous work can be as thin as one mono-layer without loss of functionality. In fact, for accumulation-channel devices only the first mono-layer is of importance with any additional material on top only working as a mechanical buffer. The pivotal ingredient for a thin-film transistor model is to treat the active layer as two-dimensional. In this case, the charge density induced in the active layer by the gate is a linear function of the local potential drop across the insulator (also called "oxide" here for historical reasons, as an inheritance from silicon technology) [1]:

$$\rho(x) = [V(x) - V_g]C_{ox} \tag{1}$$

with $\rho(x)$ and $V(x)$ the local charge density and potential, respectively at position x, V_g the uniform potential at the gate layer, independent of x, and C_{ox} the insulator capacitance density resulting from the separation of gate layer and active layer by the insulator with thickness d_{ox} and permittivity ε_{ox}, namely $C_{ox} = \varepsilon_{ox}/d_{ox}$.

In the case of pure, wide-band-gap semiconductors (wide-band-gap is defined here as a band-gap for which there is a negligible thermal excitation of carriers from valence band to conduction band at room temperature; silicon is for instance in this respect a wide-band-gap material), the charge is either free holes (p) or free electrons (n), depending on the sign of the gate bias, and the zero-bias density of them is 0. For example, for a hole-channel (negative gate bias) in an intrinsic wide-band-gap semiconductor, the substitution $\rho(x) = qp(x)$ can be made. Furthermore, the current I_x at any place in space is equal to the local charge density multiplied by the local field $dV(x)/dx$ and the hole mobility μ_p (i.e., the current is only comprised of drift current and diffusion currents are negligible), and scaled by the device width W (see Fig. 1). In other words,

$$I_x(x) = -qWp(x)\mu_p \frac{dV(x)}{dx} \tag{2}$$

and

$$p(x) = \frac{C_{ox}[V(x) - V_g]}{q}$$

The solution of this differential equation (for V_g and V_{ds} both negative) when using the correct boundary conditions ($V(L) = V_{ds}$, with L the distance between source and drain electrodes, $V(0) = 0$ and $I_x(x) = I_{ds}$ for all x) is

$$I_{ds} = -\frac{W}{L}C_{ox}\mu_p \left(V_g V_{ds} - \frac{1}{2}V_{ds}^2\right) \tag{3}$$

which is similar to the MOS-FET equations, but has the advantage that the starting point is more adequate for TFTs.

In the current work we will discuss what will happen when the condition that the zero-bias density of holes and electrons is negligible is relaxed. For this we use the following ingredients:

1. The active layer is neutral at zero-bias. This implies that there is no charge transfer between the active layer and the gate or insulator layer. In other words, they all have the same electrochemical potential.
2. All charge is free charge, free holes p and free electrons n, implying that the material is intrinsic without traps or other ways of storing immobile charge; all induced charge contributes to current. For doped semiconductors this limitation will be relaxed and charge can also be stored on the dopants by ionizing them.
3. The total charge, the sum of negative charge and positive charge follows Eq. (1), namely

$$p(x) - n(x) = \frac{[V(x) - V_g]C_{ox}}{q} \tag{4}$$

   For doped semiconductors an extra term is added to the left side of this equation to include ionized impurities, while for metals a term is added to the right-hand side representing the electron sea, as will be discussed later.
4. The relative densities of electrons and holes follow a Fermi–Dirac distribution defining a Fermi level. For all normal currents (small drain-source biases), this Fermi level is equal for electrons and holes (there is thermal equilibrium at all places and no electron–hole recombination currents exist). The product of electron density and hole density thus depends on the temperature and the band-gap of the material [3]:

$$pn = n_i^2 = N_V N_C \exp\left(\frac{-E_g}{kT}\right) \tag{5}$$

   with n_i is the intrinsic electron density, N_V the effective density of states of the valence band and N_C is the conduction band states. E_g is the electronic band-gap. Note that all units of density are "per area".
5. The current can have contributions from both electrons and holes, the first part of Eq. (2) is replaced by

$$I_x(x) = -qW[p(x)\mu_p + n(x)\mu_n]\frac{dV(x)}{dx} \tag{6}$$

The difference between these narrow gap materials and the wide band gap devices described earlier by us [1] is that in these materials electrons and holes can be present in substantial amounts *at the same place and time*, because Eq. (5) allows for that; n_i is large where for wide-band-gap materials it is negligible. Even if the wide-band-gap materials are ambipolar (with both electron and hole mobility large), they can only have electrons and holes and their associated currents at separate regions of the device. In narrow-gap materials, on the other hand, electrons and holes can coexist at the same time and place in the channel.

In the next sections the different classes of normally-on devices are described. For the transfer curves, the linear region is used. In this mode of operation, it is assumed that the drain-source bias is so small as to guarantee a homogeneous device (charge densities and electric field constant over the entire channel, independent of x). The conductance is then defined as

$$G \equiv \left.\frac{\partial I_{ds}}{\partial V_{ds}}\right|_{V_{ds}=0} = q\mu_p pW/L \tag{7}$$

For the figures, this conductance is multiplied by a small potential, for example $V_{ds} = -0.1$ V to result in transfer curves ($I_{ds} - V_g$). For the IV curves ($I_{ds} - V_{ds}$), the differential equation, defined by Eqs. (4)–(6), is solved. This is done numerically using Matlab.

Table 1
Simulation parameters used in this work (unless otherwise specified)

Parameter	value	unit
N_C	2.8×10^{16}	m^{-2}
N_V	1.04×10^{16}	m^{-2}
C_{ox}	160	$\mu F/m^2$
V_{ds}	−0.1	V
W	1	cm
L	10	μm
μ_p	3	cm^2/Vs
μ_n	1	cm^2/Vs
E_g (for narrow gap)	0.1	eV
E_A	0.2	eV
T	300	K
n_i	2.5×10^{15}	m^{-2}

3. Narrow-gap semiconductors

Narrow-gap materials, in the context of the current work, are defined as materials in which both electrons and holes exist in thermal equilibrium. Silicon, for instance, is here considered a wide-band-gap material since the room-temperature density of free charge in intrinsic silicon is much less than the charge induced by typical operating voltages. Unipolar devices are made of semiconductors where the mobility of one type of carrier is much higher than that of the other type. For most organic semiconductors, it is normally found that the hole-mobility is much higher than the electron mobility. As we have shown, low mobility in organic materials is due to a high density of traps; the intrinsic mobility of pure crystalline materials is expected to be as high as their technologically more advanced inorganic counterparts [2]. In this section we will give an example of a narrow-gap material with high hole mobility ($\mu_p = 3\,cm^2/Vs$) and zero electron mobility ($\mu_n = 0$).

The first direct obvious result of the description in the previous section is that there is free charge (both electrons and holes) and thus non-zero conductivity of the channel even at zero-bias. As an example, for a device with parameters as in Table 1, with a bad gap of 0.1 eV, the room-temperature zero-bias density of electrons and holes according to Eq. (5) is $p = n = 2.5 \times 10^{15}\ m^{-2}$ uniform over the entire channel. The conductance in the linear region (tiny V_{ds}), defined in Eq. (7) is 120 μS, resulting in a current of approximately −12 μA for a bias of $V_{ds} = -0.1$ V. In other words, the device is of the so-called "normally-on" type because a current can exist even in the absence of a (gate) bias.

The holes can be driven out of the channel by a positive gate bias. However, holes cannot be completely removed from the channel, since this would need an infinite density of electrons (Eq. (5)) and thus an infinite gate bias (Eq. (4)). For a normally-on intrinsic device, the hole density along the channel can thus be calculated from Eqs. (4) and (5):

$$p(x) = \frac{[V(x) - V_g]C_{ox}}{2q} + \sqrt{n_i^2 + \left(\frac{[V(x) - V_g]C_{ox}}{2q}\right)^2} \tag{8}$$

For small n_i this returns to Eq. (2) b. In the linear regime ($V(x) \approx 0$ and a distribution of p uniform in the channel), the bias interval at which p and thus the current goes from two times to half the zero-bias value is

$$V_g = \pm\frac{3qn_i}{C_{ox}} = \pm\frac{3q}{C_{ox}}\sqrt{N_C N_V}\exp\left(-\frac{E_g}{2kT}\right) \tag{9}$$

For the device given here, this is in the order of ±1.1 V. Fig. 2 a shows a simulation of the transfer curves for such a unipolar normally-on device. Interesting to observe is that, were the device analyzed with a classical MOS-FET model in the bias range shown, a threshold voltage of approximately 1.6 V would have been estimated at room-temperature (see the dashed line in the figure). Yet, this estimation depends on the selected bias range and tends to 0 for large gate voltages, as Eq. (8) easily demonstrates (extrapolate to $p = 0$ with n_i small compared to the other terms). The threshold voltage is not

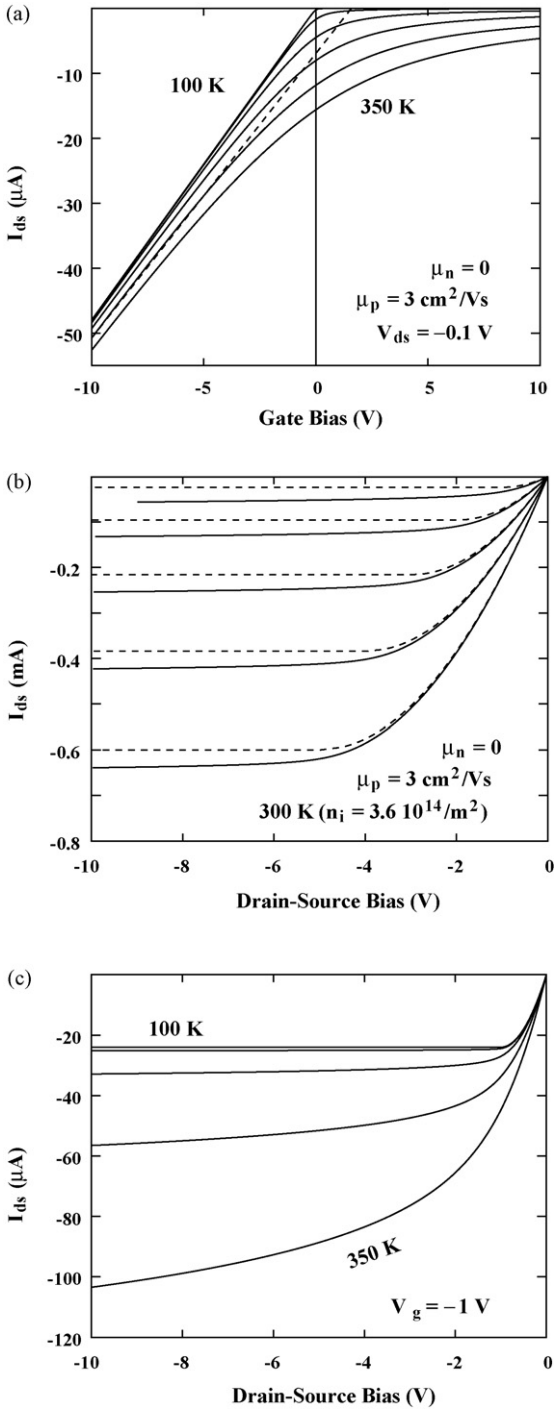

Fig. 2. Simulation of a narrow-band-gap unipolar device with parameters as in Table 1($\mu_n = 0$): (a) transfer curves ($I_{ds} - V_{gs}$) for temperatures ranging from 150 K (top) to 350 K (bottom) in steps of 50 K. The dashed line shows an attempt-to-fit a classical MOS-FET model to the behavior at $T = 300$ K, resulting in $\mu_{FET} = 2.7\ cm^2/Vs$ and $V_T = +1.64$ V. (b) Output curves ($I_{ds} - V_{ds}$) at 300 K for gate biases from −1 V to −5 V in steps of 1 V. The dashed lines show the behavior for a wide-band-gap material ($n_i = 0$). (c) Output curves ($I_{ds} - V_{ds}$) at $V_g = -1$ V as a function of temperature (100–350 K in steps of 50 K). For the lowest temperatures, the device behaves like a wide-band-gap device with a pinch-off voltage equal to V_g. For higher temperatures, the device stops showing saturation.

a device parameter for pure materials and only makes sense when traps are present [2].

The second part of Fig. 2 shows simulations of the output curves at room-temperature. They are based on a substitution of Eq. (8) into Eq. (2) and numerically solving this differential equation. Note the absence of saturation in the current. For the same reason that the channel is open at $V_g = 0$, it is not possible to completely close the channel ("pinch off"); this would need an infinite density of electrons ($p = 0$ implies $n = \infty$, according to Eq. (5)). For comparison, the dashed lines in the figure show the equivalent wide band-gap device ($n_i = 0$). Fig. 2 c shows the temperature dependence of a typical output curve at various temperatures. For the lowest temperatures, the device behaves like a standard TFT with pinch-off at $V_{ds} = V_g$, while for higher temperatures, no saturation takes place.

In ambipolar materials, mobilities of electrons and holes are comparable. Such materials were already described in the first part of this series of works, but they were limited to wide-band-gap materials. In this section we describe the narrow-gap ambipolar materials. The solution can be found by combining Eqs. (4)–(6), now with a non-zero mobility for both electrons and holes. The complexity of the differential equation prohibits its analytical solution, but a numerical solution is readily found (as all of the systems presented here). Fig. 3 a shows transfer curves at various temperatures.

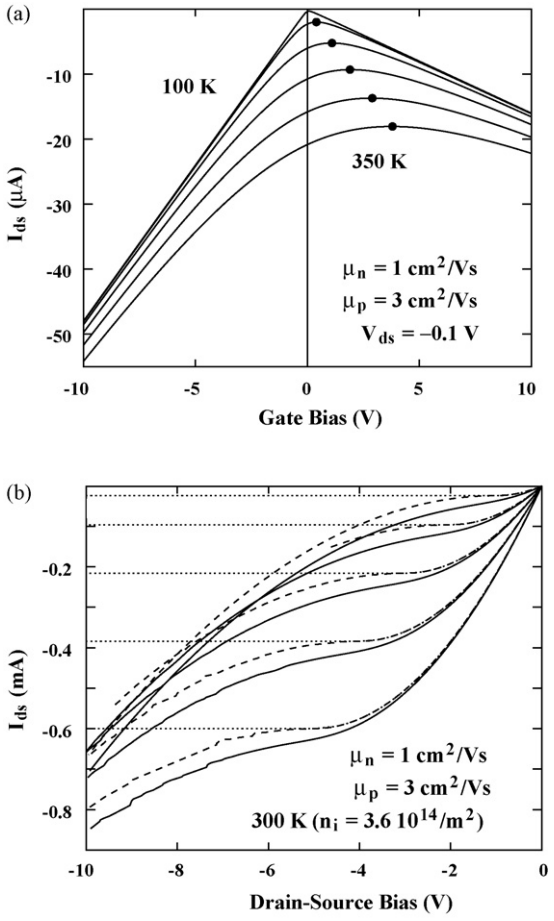

Fig. 3. Simulation of a narrow-band-gap ambipolar device with parameters as in Table 1: (a) transfer curves ($I_{ds} - V_{gs}$) for temperatures ranging from 100 K (top) to 350 K (bottom) in steps of 50 K. The full circles indicate the minimum conductance according to Eq. (10). (b) Output curves ($I_{ds} - V_{ds}$) at 300 K for gate biases from −1 V to −5 V in steps of 1 V. The dashed lines show the behavior for a wider band-gap ambipolar material (n_i 1000 times smaller) and the dotted lines represent output curves for wide-band-gap unipolar devices.

The channel in narrow-band-gap ambipolar devices cannot be completely closed, since driving out holes with the field means accumulating electrons and increases the conduction. However, the transfer curves have a minimum in the linear region. It can easily be shown that the minimum in conductance (Eq. (7)) occurs for a bias

$$V_{g,min} = \frac{qn_i(T)}{C_{ox}} \left(\sqrt{\frac{\mu_p}{\mu_n}} - \sqrt{\frac{\mu_n}{\mu_p}} \right) \quad (10)$$

and thus depends on the relative mobilities and the temperature (Eq. (5)). This point of minimum conductance is indicated in Fig. 3 a. As such, these minima can serve as rapid evaluation tools of the relative mobilities.

Again, the lack of the possibility of closing the channel goes hand in hand with the non-saturability of IV curves, as can be seen in Fig. 3 b.

4. Thick thin-film transistors

As discussed before, a thin-film transistor only needs a single mono-layer to function well [1]. A special case occurs when the transistor works in the thin-film regime – when not working in inversion as in a MOS-FET, so either intrinsic material, as discussed above, or working in accumulation in doped semiconductors, to be discussed later – but the film itself is thicker than one mono-layer. When the material is not conductive, nothing will change and normal electronic TFT behavior will be observed, as for wide-band-gap intrinsic materials. Conduction will always be in the first mono-layer and the other layers are passive buffers. However, when the material is conductive, either because of the narrow band gap, or because of doping of the material, or the layers are metallic, things change. The field-effect still occurs in the first mono-layer, but the adjacent mono-layers now form parallel conduction paths, not influenced by any bias at the gate. The field-effect is thus drowned in the parallel conductance. Once this is realized, the simulation of the behavior is obvious, yet it is still useful to illustrate this in a figure, for a quick overview. Fig. 4 shows the output and transfer characteristics for a device as used in the previous paragraph at 300 K with various numbers of mono-layers. In this simulation, each mono-layer contributes a conductance of 120 μS (or a parallel resistance of 8.4 kΩ), unaffected by the gate. As can be seen, multi-layer devices can easily be confused with narrow-band-gap devices; both cause a non-completely closing of

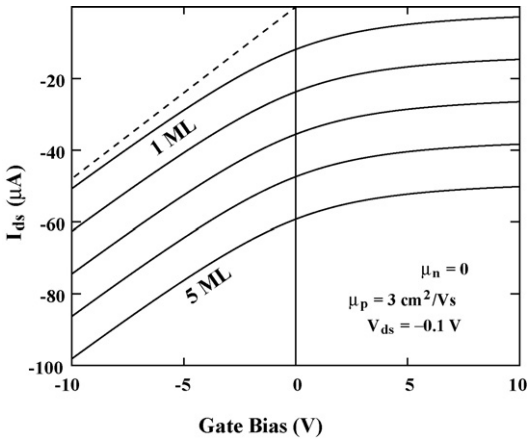

Fig. 4. Simulation of a thick narrow-band-gap unipolar device with parameters as in Table 1($\mu_n = 0$) for different thicknesses ranging from 1 mono-layer to 5 mono-layers. The dashed line shows the behavior of similar devices made of wide-band-gap materials, independent of film thickness.

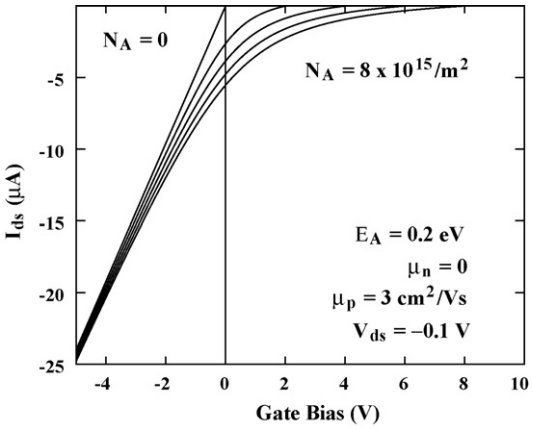

Fig. 5. Simulation of a doped wide-band-gap unipolar device with parameters as in Table 1($\mu_n = 0$) for different acceptor concentrations ranging from 0 to 8×10^{15} m^{-2} in four equal steps with energy $E_A = E_V + 0.2$ eV. The current is found as the conductance of Eq. (7) multiplied by V_{ds}.

the device at reverse bias. For comparison, the dashed line in the same figure shows the behavior of similar films made of wide-band-gap materials, which is independent of film thickness since additional layers carry no free charge and do not contribute to conductance.

In the discussion above, it was assumed that the second layer (and consecutive layers) cannot be affected by the gate. This is true up to a certain extent. Once the first layer has been depleted, the second layer starts being modified. The bias at which this starts being important however is quite large, as can be seen by checking when the induced charge becomes comparable to the density of band states. For the above device this is expected to happen at approximately $V_g = -qN_V/C_{ox} = -10$ V.

5. Doped semiconductors

Another class of conductive materials is doped semiconductors. For the same reasons as for the narrow-gap materials, devices based on these semiconductors will show conductance, even in the absence of a gate field and will thus result in a "normally-on" device. In case of a material doped with donors with density N_A at energetic position E_A this implies substituting Eq. (4) by

$$p(x) - N_A^-(x) - n(x) = \frac{[V(x) - V_g]C_{ox}}{q}, \tag{11}$$

The system is not analytically solvable, but it can easily be solved numerically. For the linear region the approximation can be made that the charge densities of Eq. (11) are constant in space (independent of x). The solution for each bias is then found by applying a zero-finding algorithm to the difference of the left side and the right side of Eq. (11) as a function of the position of the Fermi level, using Fermi–Dirac distributions for the occupancy of the levels. The conductance is then found by Eq. (7)(assuming a unipolar behavior, $\mu_n = 0$). Fig. 5 a shows a simulation of transfer curves for such a wide-band-gap doped semiconductor device. The effects are similar to the effects of narrowing the band-gap (Fig. 2), namely a normally-on behavior, but, as can be seen, for doped semiconductors the channel can be closed, namely for a threshold voltage equal to $V_T = qN_A/C_{ox}$.

Doped semiconductor TFTs, only work in accumulation, even when the material is ambipolar. When the devices are driven in inversion, the dopants are no longer compensated by free charges. This causes band bending.

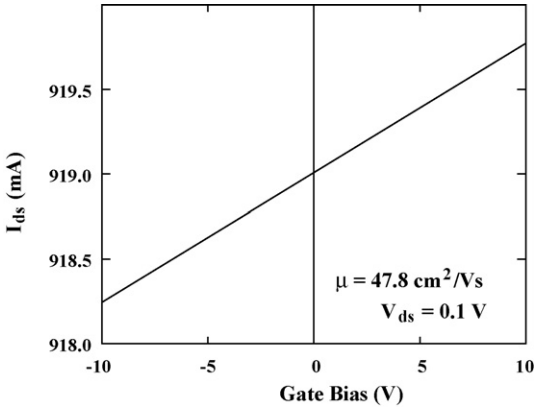

Fig. 6. Simulation of a gold–insulator–gold TFT transfer curve with parameters as in Table 1($n_0 = 1.2 \times 10^{19}$ m^{-2} and $\mu = 47.8$ cm^2/Vs).

6. Metal–insulator–metal TFT

One interesting aspect of the TFT model is that the materials are not limited to semiconductors only, as already stated in the first part [1]. As long as the active layer is thin, so that parallel conductance (current that is unaffected by the gate bias) is minimal, a device can be made with a metal for the active layer. As an example we will describe here a metal–insulator–metal TFT with a mono-layer of gold as the channel. In practice, such ideal devices are difficult to make, because the gold deposited on top of the oxide tends to form islands instead of a uniform coverage of the insulator. Yet, it may serve as a prototype for the model.

Gold has a density of 19,300 kg/m^{3}and an atomic mass of 197 g/mol (1 mol is $6.02214199 \times 10^{23}$ particles). With one free electron per atom, this gives a free-electron density of 5.9×10^{28} m^{-3}. The electrical resistivity of 22.14 nΩm then translates into an electron mobility of 47.8 cm^2/Vs (values taken from Ref. [4]), a value we will use for this exercise. A film with a thickness equal to one unit cell of the gold FCC crystal, 2 Å, has a two-dimensional electron density of $n_0 = 1.2 \times 10^{19}$ m^{-2}independent of temperature. (Neutrality is maintained by the positively charged matrix of the metal.) The local electron density in the presence of a field is then equal to

$$n(x) = \frac{n_0 + C_{ox}[V_g - V(x)]}{q} \tag{12}$$

Such a film, used in a device with parameters as in Table 1, will have a zero-bias conductance (Eq. (7)) of 9.2 S. Fig. 6 shows a sim-

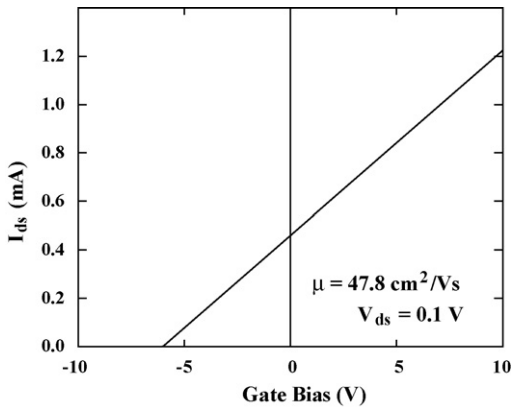

Fig. 7. Simulation of a metal–insulator–metal ("metalloid") TFT transfer curve with parameters as in Table 1($n_0 = 6 \times 10^{15}$ m^{-2} and $\mu = 47.8$ cm^2/Vs).

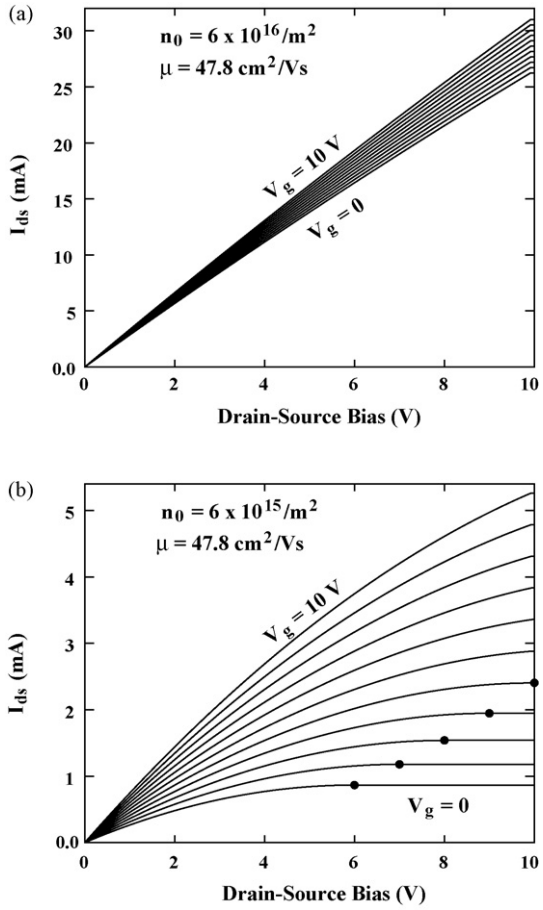

Fig. 8. Simulation of metal–insulator–metal ("metalloid") TFT output curves with parameters as in Table 1($\mu = 47.8\,\mathrm{cm^2/Vs}$), for (a) $n_0 = 6 \times 10^{16}\,\mathrm{m^{-2}}$ and (b) $n_0 = 6 \times 10^{15}\,\mathrm{m^{-2}}$. The full circles indicate pinch-off at $V_{ds} = V_g - V_T$.

ulation of a transfer curve. Because of the high zero-bias density of electrons, the relative effect of the gate field is small. However, the absolute effect, the slope of the transfer curve, yields the same mobility given above. For the same reason, the bias needed to close the channel is large, $V_T = -qn_0/C_{ox}$, and is of the order of 12 kV; impossible to attain in practice. The same voltage is needed at the drain to pinch-off the channel there. In other words, output (IV) curves do not saturate and remain linear for a very large range of voltages, with relative tiny field effect.

Organic devices may have density-of-states that are much lower than pure gold devices, even when the materials are metallic. Next we make a simulation of metallic behavior (half-filled band), but with much smaller electronic state density, though with the same charge carrier mobility of $47.8\,\mathrm{cm^2/Vs}$. We call this a metalloid behavior to distinguish it from pure metallic behavior. As can be seen in Figs. 7 and 8, when the density of states diminishes, the device behaves more and more like typical semiconductor thin-film transistors. For a zero-bias electron density of $n_0 = 6 \times 10^{15}\,\mathrm{m^{-2}}$, the bias to close the channel is $V_T = -qn_0/C_{ox} = -6$ V (Fig. 7). The output curve (Fig. 8b) thus saturates at a pinch-off voltage of $V_P = V_g - V_T$.

7. Summary and conclusions

In this work, thin-film field-effect transistors were described that are based on materials that have non-zero room-temperature conductivity. When such materials are used in TFTs, they result in so-called normally-on devices. They can be divided into three groups: (i) narrow-gap semiconductors (unipolar and ambipolar), (ii) doped semiconductors and (iii) metals. Each has its own characteristic behavior. Moreover, when the film is thick (more than one mono-layer), such normally-on devices show reduced relative field effect.

Acknowledgements

This work has been financed by the Portuguese National Foundation of Science and Technology, through projects POCTI/FAT/47956/2002 PTDC/FIS/65319/2006 and research unit no. 631, CEOT.

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