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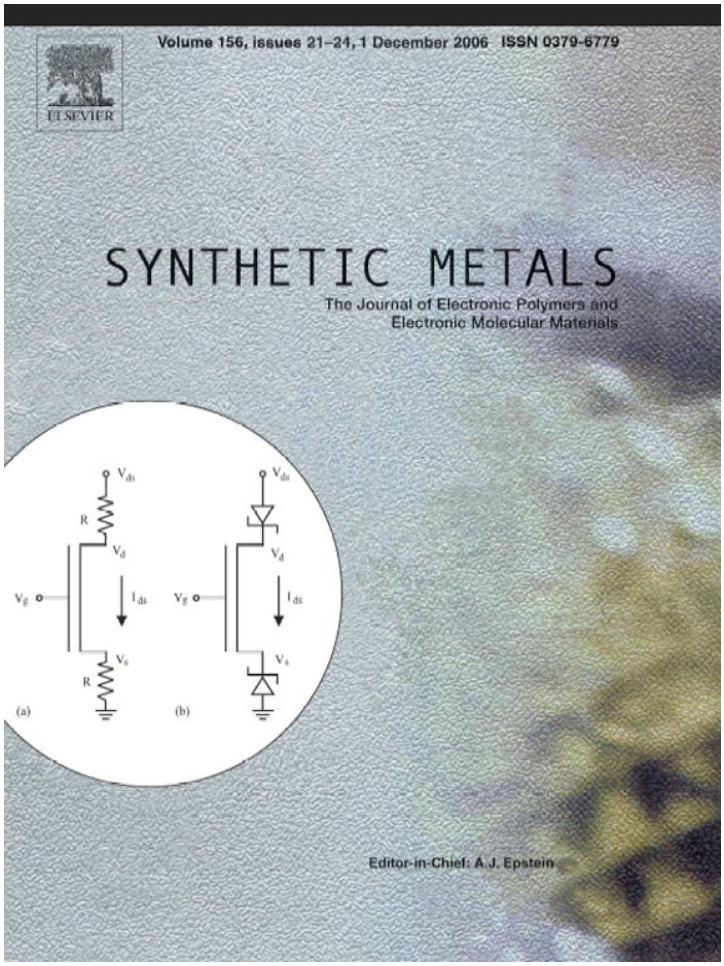

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Modeling electrical characteristics of thin-film field-effect transistors I. Trap-free materials

P. Stallinga*, H.L. Gomes

Universidade do Algarve, FCT, Campus de Gambelas, Faro, Portugal

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Abstract

A new analytical model is developed for thin-film field-effect transistors (TFTs). The active layer of the devices is considered purely two-dimensional. In the first part, the basic model is developed for intrinsic materials. It is demonstrated that it accurately describes the electrical characteristics and elucidates on the physical meaning of the device and material parameters, such as threshold voltage and sub-threshold current. It also clarifies the nature of so-called contact effects, often used in literature to explain non-linear *I–V* curves. Furthermore, ambipolar devices are treated.
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Keywords: Thin-film field effect transistors; Amorphous silicon; Organic semiconductors; Sexithiophene; Two-dimensional electronics; Contact effects

1. Introduction

In spite of the rapid growth of interest in organic electronic materials, the ever-increasing quality of the materials and devices, and the resulting unique devices [1–3] – including ambipolar devices needed for logic circuits [4] – the debate as to the processes governing and limiting charge conduction is not yet settled. Often, the carrier mobility is bias dependent [5–9], which seems difficult to explain in conventional theories. Another example is the discussion between hopping and band conduction. Apart from this, there is the question of the workings of the device. It is common practice to fully apply the conventional inversion-channel metal-oxide-semiconductor field-effect transistors (MOS-FET) model [10] to the thin-film field-effect transistors (TFT) [11]. This is surprising considering that inversion has not been observed in organic transistors. The majority of the models proposed in the literature are based on the three-dimensional model developed for inorganic MOS-FETs. The Thiais group has added a trap model, known as multi-trap-and-release (MTR) model to simulate the experimental *I–V* and transfer curves [11], while the Bell-Labs group has proposed a model in which a constant mobility is assumed in a trap-free material, but with the concept of contact resistance [12]. In the current work we first derive a simple model for TFTs that can adequately explain the basic *I–V* and transfer curves. The model is found by removing from existing theories everything that is not needed to explain the TFT behavior. A remarkably simple and yet fully functional theory emerges. Then we introduce perturbations to the model, such as the effects of the contacts and ambipolar devices. In the second part traps are added to the system and it is easily shown how they explain the temperature and bias dependence of current and mobility and transient behavior. The device described is a p-channel FET, with organic materials in mind, but the model is equally applicable to n-channel FETs and other materials, such as (amorphous) silicon, with the adequate changes of signs and symbols.

2. Background

Fig. 1 shows a cross-section of a thin-film FET with the nomenclature used in the current work. The device consists of a conductor called the gate (made of metal or a highly doped semiconductor) an insulating layer (which we will call the oxide layer

* Corresponding author. Tel.: +351 969541198; fax: +351 289800030.
E-mail address: pjotr@ualg.pt (P. Stallinga).

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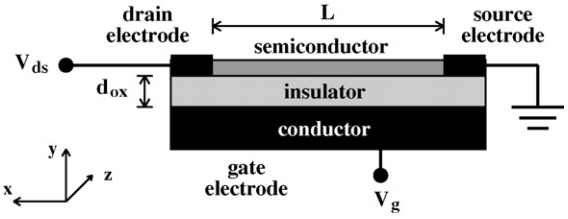

Fig. 1. Cross-section of a thin-film FET showing the nomenclature used in the current work.

throughout this work, as an inheritance from silicon technology) of thickness d_{ox} (resulting in capacitance density $C_{ox} = \varepsilon_{ox}/d_{ox}$, with ε_{ox} the permittivity of the insulator material) and a semiconducting layer that accommodates the channel of charged carriers and can thus be called the active layer. The basic working of the field effect transistor is that charge density in this layer and thus its conductivity can be modulated by a tension at the gate relative to the semiconductor. The charges are injected and collected by the source and drain electrodes, respectively. Observable external electrical quantities are: I_{ds} the drain–source current, V_{ds} the drain–source voltage and V_g the gate–source voltage. The leakage currents, such as drain–gate or gate–source, are considered zero.

It is standard practice in literature to use textbook inversion-channel metal-oxide-semiconductor field-effect transistor (MOS-FET) theory to describe the behavior of organic FETs [11]. There are two reasons why this might be inappropriate. First, the real devices are, without fail, thin-film FETs (TFT) and as such do not have a bulk region. Apart from reducing the four-terminal MOS-FET devices to a three-terminal TFT from an electronics point of view, the main concern is that a TFT, without a bulk region, cannot accommodate a band bending. Second, organic TFTs are all accumulation-channel FETs. In this situation, in the absence of localized states (donors) to store immobile positive charge, no band-bending can be be maintained, even if the active layer is thick. Summarizing, the thick semiconductor in a standard MOS-FET can accommodate band bending and will have band bending in inversion mode. Charges induced by the gate are then not all located close to the interface and a complicated charge-voltage and hence current-voltage relation results. In a thin-film FET, or in general an accumulation-type FET, all induced charge is necessarily close to the insulator and the charge–voltage relation is always simply:

$$\rho(x) = \left[V(x) - V_g\right] C_{ox} \tag{1}$$

with ρ and V the local charge per area and voltage in the channel, respectively. This charge in a TFT might still be either mobile or immobile, though. The consequences of immobile charge will also be discussed in this contribution. To give an idea of how thin the active layer in a TFT can be and still work properly: for a silicon based device, with -1 V at the gate relative to drain and source and an oxide thickness of $d_{ox} = 200$ nm, the induced charge is 0.17 mC/m^2. With a density of states of N_V of 1.04×10^{19} cm^{-3} and assuming continuity, this can fit into 1 Å; less than the height of a monolayer. The TFTs have thus effectively two-dimensional charge distributions. This explains why, as has been shown, for organic FETs only the (quality of the) first monolayer matters. At best, the consecutive layers help to stabilize the integrity of the first layer, in terms of diffusion of impurities and crystallinity.

For a standard MOS-FET, the assumption is made that the induced free charge in the channel is linearly depending on the gate bias. This is because, once the channel has been formed, all the charge induced by the gate is free charge. This in turn is caused by the type of semiconductor used in FETs. For traditional materials, viz., Si or GaAs, the acceptors and donors introduce shallow levels, which are consequently all ionized at all operational temperatures. In organic semiconductors, the acceptor and donor states are very deep and abundant. As a result, even at room temperature, not all levels are ionized and temperature and bias can change the degree of occupancy. As we will show, the as-measured mobility does not change because of an increased depth of the acceptor level. On the other hand, traps, that differ from acceptors in that they can be neutral or positively charged, have a severe effect on the electrical characteristics of the device. This is demonstrated in the second part of the work.

This article is organized in the following way. First we will derive equations for the basic operation of a TFT. Then we will discuss the differences and perturbations to the model, including contact effects and traps. As a starting remark, the units of densities used are all "per area". This includes the charge densities, carrier densities and densities of states. This might cause some confusion, especially when the same symbols are used as for their three-dimensional counterparts, for instance, N_V, the density of valence band states. In those cases they are imagined to be multiplied by the effective thickness of the active layer to arrive at the two-dimensional values.

3. Basic model

It is easy to show that the equation for currents of a MOS-FET is also applicable to thin-film FETs. In the case of a TFT the thickness of the channel is constant, but the density of charges p inside the channel varies from one electrode ("source", $x = 0$) to the other ("drain", $x = L$). To calculate the currents through the device, we have to understand that, locally, the current $I_x(x)$ at a certain point x in the channel is equal to the local induced charge, $C_{ox}[(V_g - V_t) - V(x)]$, multiplied by the carrier mobility μ, the field felt by the charges, $\mathrm{d}V(x)/\mathrm{d}x$ (only drift current considered, see comment later), and the channel width W. In other words, we have the following differential equation:

$$I_x(x) = qWp(x)\mu\frac{\mathrm{d}V(x)}{\mathrm{d}x}, \qquad p(x) = \frac{C_{ox}[V(x) - (V_g - V_t)]}{q} \tag{2}$$

V_t is the threshold voltage, which will be discussed later in a separate section. However, an important difference with standard FET models is that V_t is not related to donor or acceptor concentrations. The threshold voltage can only deviate from zero in the presence of traps. With boundary conditions $V(0) = 0$, $V(L) = V_{ds}$, and $I_x(x) = I_{ds}$ for all x, the solution is

$$I_{ds} = -\frac{W}{L}C_{ox}\mu\left[(V_g - V_t)V_{ds} - \frac{1}{2}V_{ds}^2\right] \tag{3}$$

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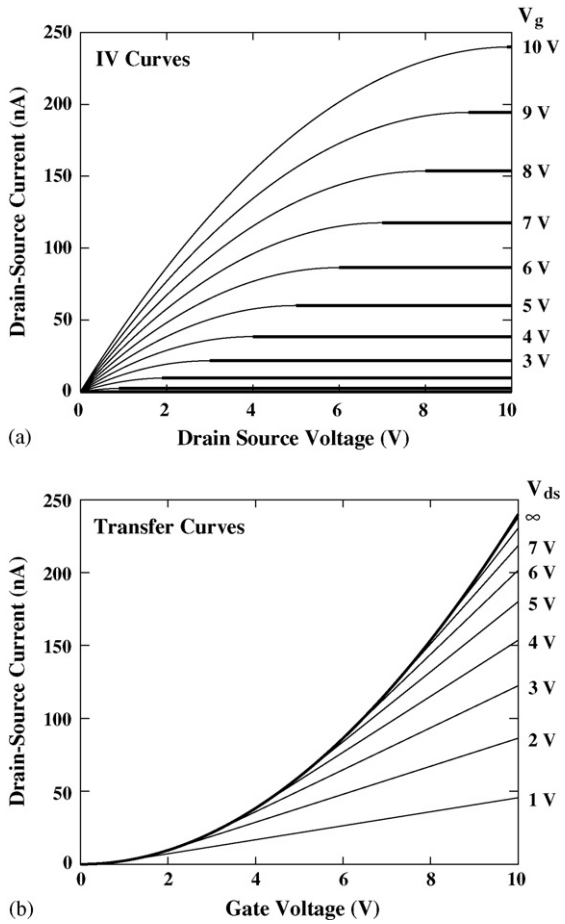

Fig. 2. (a) *I–V* curves (I_{ds} vs. V_{ds}) of an ideal thin-film FET resulting from Eq. (3) (thin lines). (b) Transfer curves for same device. The parameters are given in Table 1 . Absolute values for current and voltage. Thick lines indicate the saturation regime.

V_{ds} and V_g both negative. This equation for TFTs is very similar to the equation for MOS-FETs [10]. The only prerequisite is (low) ohmic contacts. The effects of the contacts will be discussed later. The equation is valid up to $V_{ds} = V_g - V_t$. After that, saturation starts in: a region close to the drain is below threshold voltage and is devoid of charges. When the sub-threshold conductivity is (close to) zero this region can be infinitely small and still absorb all of the above-saturation voltage $V_{ds} - (V_g - V_t)$. In this way, the charge and voltage distribution across the device (except for an infinitely thin zone) is independent of the drain–source voltage and hence the current is constant at $I_{ds} = -(1/2)(W/L)\mu C_{ox}(V_t - V_g)^2$. Fig. 2 shows the electrical characteristics of an ideal TFT.

When the sub-threshold conductivity is not zero, the above-saturation voltage can only be supported over a finitely thick zone (l) which depends on the voltage. The remaining voltage drop $V_t - V_g$ then occurs in a region that is not of constant width but shrinks to $L - l$ for increased V_{ds}. The result is that the saturation current is not constant but continues to increase for higher drain voltages. Ergo, there is a direct link between the sub-threshold current and the saturation behavior. Devices having a sub-threshold current will also exhibit *I–V* curves that do not saturate. This reasoning is equal to the one used to describe saturation behavior in the MOS-FET model.

For low voltages, the quadratic term in V_{ds} disappears from Eq. (3) and this is called the linear region. Conventionally, the mobility of an FET is defined via the derivative of a transfer curve ($I_{ds} - V_g$). Using Eq. (3) for small V_{ds}:

$$\mu_{FET} \equiv -\frac{L}{WC_{ox}V_{ds}}\frac{\partial I_{ds}}{\partial V_g} \tag{4}$$

where the subscript FET is used to distinguish it from mobilities measured by other techniques such as time-of-flight (ToF) [13–17], Hall effect, or delay of luminescence [18]. For various reasons, which will be described in the second part, for an organic TFT, the as-measured mobility can depend on things such as the temperature and the bias and can substantially deviate from mobilities measured with other techniques.

4. Effects of the contacts

In organic TFTs, often non-linearities in *I–V* curves are observed[19–24]. The argumentation is using the generic term "contact effects" [19,25–28]. In an FET there might be two possible contact effects, namely contact resistance [26,29–35] and contact Schottky barriers [36–45] (note that the references are far from being exhaustive). The first might be caused by the formation of a high resistive area in the vicinity of the drain and source electrodes. This can then impede carrier injection. A standard procedure for extracting this resistance is by measuring the device resistance as a function of channel length and extrapolating to zero [30,26,29,34,35]. This method requires an easy access to a large number of devices prepared under identical conditions and is rather time consuming. Later we will present a faster way of determining the contact resistance.

On the other hand, when a metal is brought into intimate contact with a semiconductor, usually a depletion layer is formed at the interface [10]. When their respective work functions are different, a Schottky barrier results that limits charge carrier injection. Note that the work function of the semiconductor is here defined as the electron affinity plus the Fermi-level depth, or, in other words, the distance between the vacuum level and the Fermi-level. Now we will demonstrate the effects of both type of contacts on the electrical characteristics.

Fig. 3 shows a circuit of an FET with contact resistances R at the source and the drain. For simplicity sake, these are considered to be of equal magnitude, although the results are not much different when this restriction is abandoned. Fig. 4 shows the simulation of plots for different gate biases. For R equal to zero, the ideal *I–V* curves emerge. When increasing the contact resistances, two things occur. First, the curves pinch together, and second, a tiny curvature becomes visible. This curvature is convex (sub-linear); contrary to what normally observed experimentally. This should not have come as a surprise. After all, an FET is a trans-*resistor*. Once the resistance of the channel is programmed by the gate, the *I–V* curves follow a simple electronics Ohms law. The small positive curvature is caused by the "voltage stealing" effect; a small voltage is added to the source ($\Delta V_s = I_{ds}R$), which diminishes the gate–source poten-

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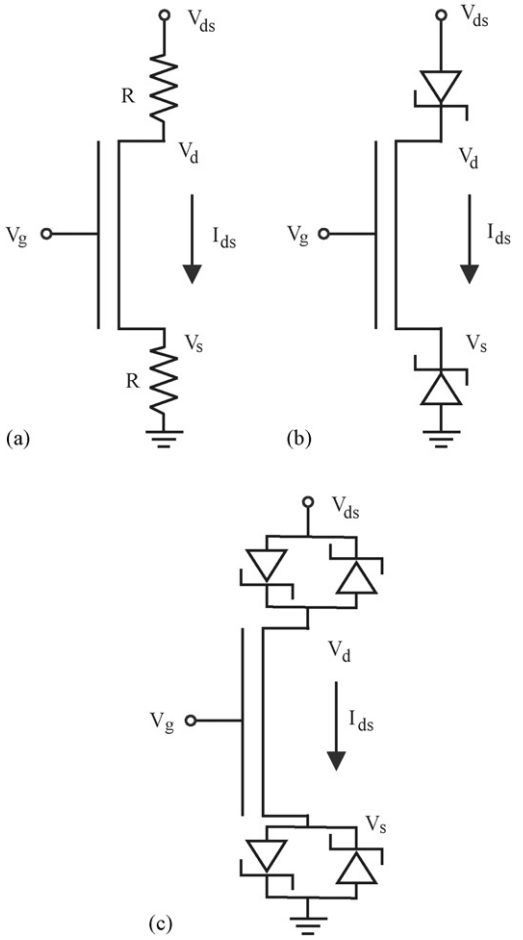

Fig. 3. Model of an ideal FET with resistances R (left), Schottky barriers (middle), or anti-parallel Schottky barriers (right) at the drain and source contact.

tial drop and thus closes the channel slightly and increases the FET resistance. The same effect causes a slight earlier onset of saturation as careful analysis of the figures shows. For very high contact resistances, the curves become independent of gate bias, as shown in Fig. 4. This is easy to understand; the currents are now totally limited by the contact resistances and the FET channel resistance is insignificant. The *I–V* curves for various gate biases become superimposed. The important conclusion that emerges is that contact resistances can explain curve crowding and sub-linear *I–V* curves. In contrast, it is often reported that experimental transistor curves show supra-linear behavior. It still be shown later that this supra-linear behavior can only be explained by including traps in the model.

Fig. 5 shows transfer curves for different contact resistances. It is clear that for higher resistances, the curves show a tendency to saturate. This is because the total resistance for high bias at the gate approaches the contact resistance and this limits the current. The maximum current is $I_{ds} = V_{ds}/2R$ for $V_g = \infty$ and this provides a rapid and reliable way for determining R requiring only a single device. Even for other models of the FET, with, for instance, bias-dependent mobility, this picture will not change substantially; in case of contact resistance, the transfer curves saturate, in the linear region, as shown in Fig. 5, as well as in the saturation region.

Alternatively, the charge injection might be limited by Schottky barriers at the electrodes. This, at first sight might seem to explain the supra-linear behavior seen in the *I–V* curves, since currents of a junction grow exponentially with bias. Indeed, many authors use such ideas to explain non-linear effects seen in the *I–V* curves. However, one must not forget that when one side (drain or source contact) is in forward bias ($I_{ds} = I_0[\exp(qV/kT) - 1]$), the other side is in reverse bias ($I_{ds} = I_0[1 - \exp(qV/kT)]$), with V the voltage drop at a contact. See Fig. 3b for the equivalent electrical circuit. The maximum current is thus the reverse-bias saturation current I_0. More precisely, not ignoring either the forward or reverse biased barrier, the currents follow:

$$I_{ds} = I_0 \tanh\left(\frac{qV_{ds}}{kT}\right) \tag{5}$$

with k Boltzmann's constant, T the absolute temperature and q the elementary charge. For small voltages of the argument, tanh is a linear function. For $V_{ds} \gtrsim 3kT/q$ (80 mV at 300 K), the dependence of the current on V_{ds} disappears, indicating that these barriers, although possibly limiting the current, can never cause non-linearities in the $I_{ds} - V_{ds}$ curves over a large voltage range. Including an ideality factor n in the equation can only stretch this by a factor n, with n normally in the range 1–5. Moreover, the currents are independent off the gate bias. See Fig. 6 for a visual comparison of the basic FET model with a Schottky-barrier-limited model. Sometimes in literature, especially authors describing electronic (SPICE) models of the device use a model of an FET with double, antiparallel diodes at the electrodes [34,46], see Fig. 3c. This results in a good description of the devices, but lacks physical basis. A combination of a Schottky barrier at the forward-biased contact and a resistance at the counter-electrode might do the trick, but also here the explanation becomes awkward. Another effect at the contacts might be tunneling diodes [47]. As shown before [10], the currents are of the form $I = I_t[\exp(qV/kT) - 1]$, with I_t exponentially depending on the barrier height and tunneling distance D, $I_t \propto \exp(\alpha\phi_{Bp}/D)$. The same reasoning for the Schottky barriers above can be applied to tunnel barriers. We conclude that Schottky barriers cannot explain non-linearities in the *I–V* curves experimentally observed.

The above analysis is based on a two-terminal geometry, by temporarily ignoring the presence of the gate and imagining Schottky barriers as electronic components added at the contacts. This picture is far from adequate. When the gate is included, the designation "Schottky barrier" is a misnomer. In a Schottky barrier, the distribution of charge and voltage is governed by space charge and band bendings through Poisson's equation, something that is allowed when the device can be considered stretching to infinity in the dimensions (y, z) perpendicular to the current (x). The actual area of the interface then only enters as a scaling parameter. The presence of the gate breaks this symmetry and the reduced thickness further undermines the validity of the Schottky-barrier analysis. As discussed in the beginning of this work, in a TFT, the charge at any point is determined by the local voltage relative to the gate. We will now present a model

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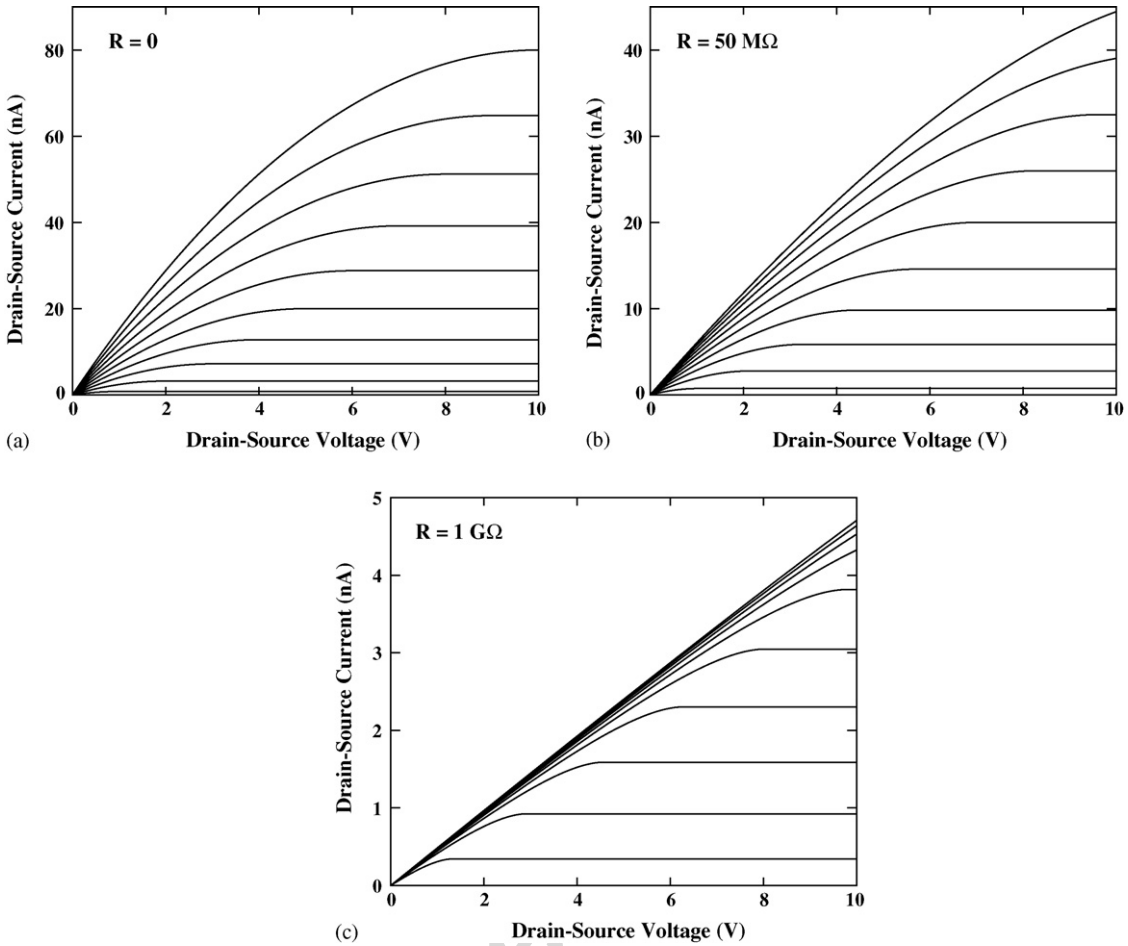

Fig. 4. Simulations of *I–V* curves of FETs with contact resistance *R* as indicated for gate bias from 1 to 10 V. Parameters as in Table 1. Absolute currents and voltages shown.

for an accurate description of the effects of metal–semiconductor contacts in TFTs, that is based on this idea.

As a starting point, we observe that the structure, at first glance, seems similar to MOS-FET devices with pn-junctions at the electrodes. There, n-type (p-type) electrodes are injecting electrons (holes) into the electron-channel (hole-channel) in a p-type (n-type) layer. In this case, no non-linearities result, as demonstrated in the chapter on MOS-FETs of the book of Sze [10]. In these devices the electrodes are made of the same material (with different doping) as the channel. When a bias is applied, at the threshold voltage two effects occur simultaneously: (1) free charge is induced in the channel; (2) the

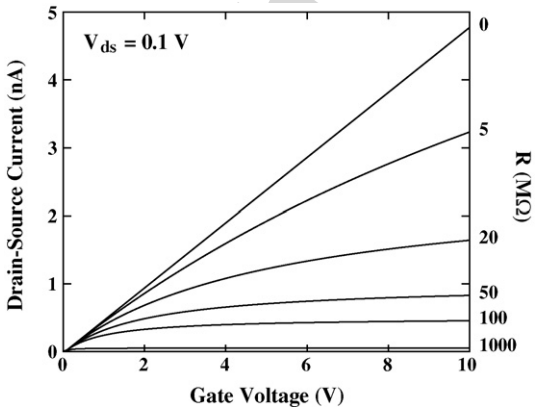

Fig. 5. Transfer curves for various values of contact resistance. Parameters of the ideal FET given in Table 1. Absolute currents and voltages shown.

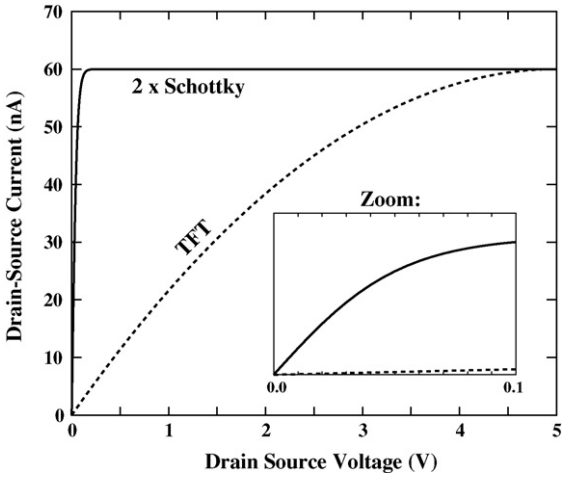

Fig. 6. Comparison of the Schottky-barrier-limited model of Eq. (5) (solid) with the basic TFT model of Eq. (3) (dashed). The latter saturates typically after some volts whereas the former already saturates after $V_{ds} \gtrsim 3kT/q$ (80 mV at 300 K). The inset shows a zoom-in at the low voltage region. Parameters of the simulation are give in Table 1.

pn-junctions at the electrodes disappear. When the charge in the channel is exactly equal to the charge density in the electrodes (at V_t), by definition, the bands on both sides of the barrier have aligned. For organic thin-film FETs these effects might occur at different voltages, since the electrodes and the active layer are not made of the same material. The threshold voltage for creating a charged channel is zero, as shown above, but at zero bias, the (Schottky) barriers might still exist, limiting the current. A fundamental difference between a TFT and an MOS-FET is in the dimensions. Fig. 7a shows the energetic band diagram before contact, E_C and E_V are the conduction band and the valence band in the semiconductor, respectively. In the semiconductor the Fermi level E_{Fs} is at mid-gap. Assuming the Fermi level in the metal E_{Fm} to be lower, $\Delta E_F \equiv E_{Fs} - E_{Fm} > 0$, the following happens upon making contact: electrons flow from the semiconductor to the metal, or holes from the metal to the semiconductor. These holes p redefine the Fermi level in the semiconductor to the new value E_{Ff} according to the Fermi–Dirac distribution (simplified to the Boltzmann distribution):

$$p = N_V \exp\left[\frac{E_V - E_{Ff}}{kT}\right] \tag{6}$$

with N_V the effective density of valence band states. This accumulated charge in the channel implies a voltage relative to the gate, determined by Eq. (1):

$$\Delta V = \frac{qp}{C_{ox}} \tag{7}$$

The two effects, moving of the Fermi-level and increasing of the voltage caused by the charges, sum up to align the Fermi levels across the device:

$$q\Delta V + (E_{Fs} - E_{Ff}) = \Delta E_F \tag{8}$$

Combining Eqs. (6)–(8) we find a voltage drop of

$$\Delta V = \frac{kT}{q} W\left(\frac{q}{kT} A\right) \tag{9}$$

With W the Lambert-W function [48], and A equal to

$$A = \frac{qN_V}{C_{ox}} \exp\left(\frac{E_V - E_{Fm}}{kT}\right) \tag{10}$$

The voltage drop ΔV from the metal contacts to the semiconductor channel is assumed to occur abruptly, as in metal–metal contacts. In the absence of donors and acceptors that can store immobile charge, or in accumulation, no band bending can exist. Or better, any band bendings are caused by mobile charge in the band and with the huge DOS of band states, the depletion width can effectively be considered zero, as in metal–metal contacts.

Two extreme cases are worth to highlight. When the Fermi level in the semiconductor does not change much by the accumulated charge, $(E_{Fs} - E_{Ff}) \approx 0$, for example in doped semiconductors, the effect is nearly completely absorbed by the interface, $\Delta V \approx \Delta E_F/q$ and this can be substantial (in the order of volts, depending on the starting difference of Fermi levels). In the other extreme case, when only a small accumulation of charge is needed in the channel to move the Fermi level substantially, in the case of intrinsic semiconductors, the equation reduces to $(E_{Fs} - E_{Ff}) \approx \Delta E_F$ and $\Delta V \approx 0$. It is interesting to compare this to the voltage profiling experiments carried out by Bürgi et al. [49], in organic thin-film transistors. They report on a small voltage drop at the contacts, even in the absence of bias, exactly as predicted above. Substituting the voltage of the channel into Eq. (1), gives the zero-bias charge density in the channel. The conclusion is that even without a bias it is possible to have free charge in the channel. In other words, the device is a normally-on FET with a positive threshold voltage. The charge density and the threshold voltage can be tiny, though.

At the same time, the residual barrier at the interface, $q\phi_{Bp}$ is equal to the final depth of the Fermi level, $E_{Ff} - E_V$, as can be seen in Fig. 7. According to Eq. (6), this residual barrier height is in the order of some tens of meV, and depends on the free

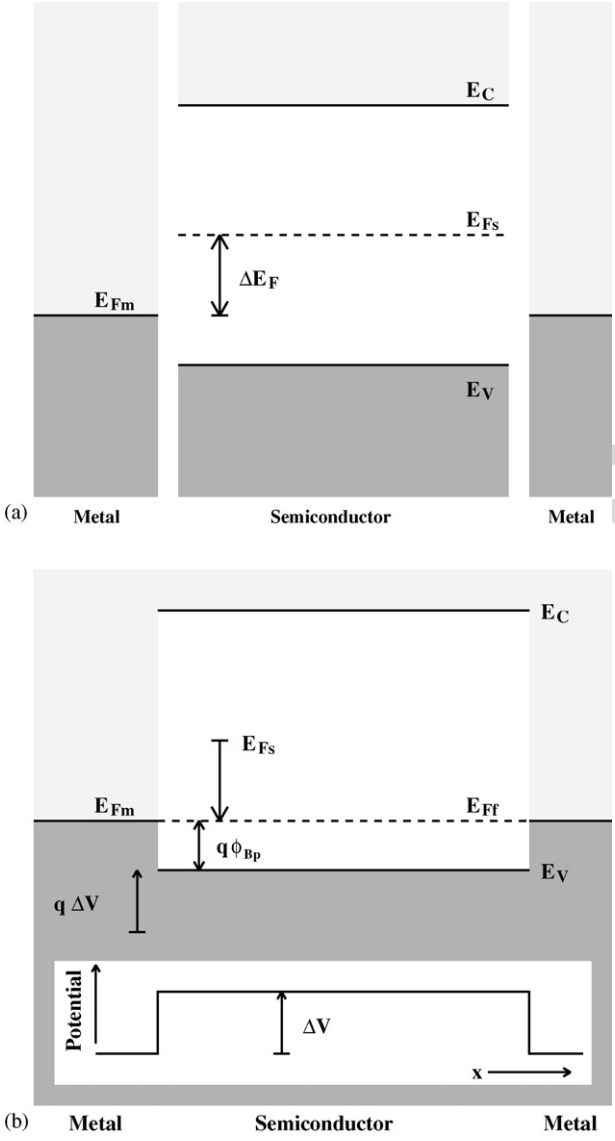

Fig. 7. Schematic energy diagram of a metal-contact TFT before (a) and after (b) contact. The parameters are—E_{Fm}: Fermi level in the metal; E_{Fs}: Fermi level in semiconductor before contact; E_{Ff}: Fermi level in semiconductor after contact; E_C and E_V: conduction band and valence band, respectively; ΔV: voltage drop at the interface and equal to the voltage in the channel, as shown in the inset.

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Table 1
Simulation parameters used in this work (unless otherwise specified)

Parameter	Value	Unit
N_V	1.04×10^{16}	m^{-2}
C_{ox}	160	$\mu F/m^2$
V_{ds}	−0.1	V
W	1	cm
L	10	μm
μ_0	3	$cm^2\,V^{-1}\,s^{-1}$
E_g	1.12	eV

carrier density, and thus on the gate-bias, and the temperature:

$$q\phi_{Bp} = E_{Ff} - E_V = kT\,\ln\left(\frac{C_{ox}(\Delta V - V_g)}{qN_V}\right) \tag{11}$$

As an example, for a device with parameters as in Table 1, at $T = 300\,K$, $\Delta V - V_g = 1\,V$, the barrier height is 61 meV. Relevant, in view of this, is the report of a gate-bias-dependent contact resistance in pentacene TFTs with an activation energy of 80 meV [33], which we attribute to the residual barrier $q\phi_{Bp}$.

The effects described above are caused by the fact that before contact the Fermi level in the semiconductor was higher than in the metal. Using the same reasoning, a negative charge can accumulate when $E_{Fs} < E_{Fm}$, and a negative threshold voltage exists, resulting in a normally-off FET. Note that if these electrons have low mobility, it may take time to establish this threshold voltage. When acceptors are introduced into the system, the picture stays the same, as long as the device is in accumulation, meaning positive charge or neutrality everywhere. When the device goes, for reasons of bias or contact effects, into depletion or inversion, with negative immobile charge on the acceptors, the picture changes, since then band bendings and space charge can start playing a role.

After contact, there is a residual barrier with height $q\phi_{Bp}$ equal to the difference in Fermi level in the metal and valence band V_B in the semiconductor. It is important to point out the difference with a Schottky barrier. There, the bulk Fermi level and thus the barrier height is constant and depends only on the workfunctions of the materials, whereas in an FET the Fermi level in the bulk, and thus the barrier height, can be programmed by the gate. When free charge is present in the channel, the Fermi level (in the semiconductor equal to the metal) is close to E_V and the barrier is virtually zero (some tens of mV). No substantial barrier can exist above threshold voltage. It is unlikely that the barrier is the current-limiting factor.

5. Threshold voltage and sub-threshold current of intrinsic TFTs

It is common practice to use the threshold voltage and the sub-threshold current as device-evaluation parameters [10]. They are often used to extract information about impurity concentrations, traps and interface states. In the context of the two-dimensional model described above, it is important to understand the physical meaning of these device parameters. In this section, we will analyze the trap-free device based on intrinsic materials and show that the threshold voltage and sub-threshold current do have different behavior compared to the conventional MOS-FET models.

As discussed in the previous sections, the threshold voltage in TFTs is zero because, in the absence of localized states, originating from donors, acceptors or defects, all induced charge is necessarily mobile. In the second part we will show how traps can cause a non-zero threshold voltage. Here we will continue by analyzing the sub-threshold current of trap-free devices.

In MOS-FETs, the sub-threshold current is exponentially depending on the gate-bias as well as the drain–source bias. The reason for this is that below threshold the free carrier density is exponentially depending on the local bias. (The energetic distance between band edge and Fermi level is linearly depending on the voltage drop across the insulator and the free carrier concentration is depending exponentially on this distance.) In the linear region, the potential at the drain is slightly smaller than at the source. Therefore, p is exponentially smaller at the drain compared to the source. Such a high gradient in density causes the diffusion current to dominate. (Drift currents are still insignificant because the densities are still too small.) The gradient and the current thus depends exponentially on V_{ds} and V_g. The current is proportional to the difference in density at the source and the drain, $I_{ds} \propto \exp(V_g) - \exp(V_g - V_{ds}) \approx \exp(V_{ds})\exp(V_g)$, which leads to the equation normally found in textbooks. Above threshold, the densities depend linearly on the potential and drift currents exceed the diffusion currents.

Because thin films do not have space to accommodate band bending, resulting in the basic equation (1), the charge density does not depend exponentially on the potential as in MOS-FETs, but always linearly. To make a crude analysis of the sub-threshold current in TFTs we have to bring electrons into the model and make three assumptions: (1) The charge, electrons and holes, is homogeneously distributed over the channel thickness. This is either the thickness of the active layer or the diffusion length, whichever is smaller. For the calculation we use a thickness of $d = 1\,nm$. (2) The thermal equilibrium equation of electrons and holes is maintained:

$$np = n_i^2 = N_V N_C\,\exp\left(-\frac{E_g}{kT}\right) \tag{12}$$

with n_i the intrinsic electron density (note again that all units of density are "per area", including n_i, N_V and N_C) and E_g the electronic band gap. For small currents this holds. (3) The electrons are immobile and do not contribute to current [50] (for the ambipolar devices discussed later this third condition will be abandoned). Then we have to imagine that the induced charge is caused by the the difference between p and n, Eq. (1) becomes:

$$n - p = \frac{V_g C_{ox}}{q} \tag{13}$$

The solution of Eqs. (12) and (13) is

$$p = -\frac{V_g C_{ox}}{2q} + \sqrt{n_i^2 + \left(\frac{V_g C_{ox}}{2q}\right)^2} \tag{14}$$

For large negative voltages $p \gg n_i$ this reduces to the original form; the currents are proportional to the gate voltage. For large

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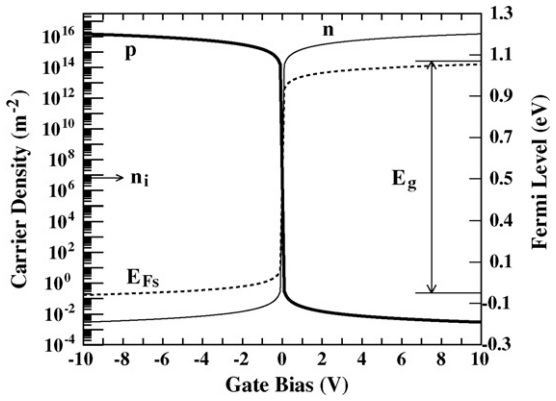

Fig. 8. Carrier densities, p and n (solid lines), and the position of the Fermi level (dashed line) as a function of bias. Assuming electrons have zero mobility, the current in the linear region is proportional to p. Parameters as in Table 1.

positive voltages, the sub-threshold current can be shown to be:

$$I_{ds} \propto p = 2\left(\frac{qn_i}{V_g C_{ox}}\right)^2 \tag{15}$$

i.e., not exponential. To give an idea, the interval at which the currents goes from two times to half the zero-bias current is

$$V_g = \pm\frac{3qn_i}{C_{ox}} \tag{16}$$

and is in the order of nano-volts. Fig. 8 shows the position of the Fermi level and the charge densities as a function of bias. The example is for a silicon TFT. For materials with wider band-gap, such as most organic materials, the sub-threshold current is even much less. Therefore, for all practical purposes, the sub-threshold current can be ignored.

6. Ambipolar devices

In the preceding text it was assumed that the mobility of the free electrons was so low as never to contribute to current $\mu_n \approx 0$, even when electrons are injected into the conduction band [50]. For this reason, when the gate bias is positive, and at no place in space free holes exist, but only immobile electrons, no current is possible. We will now extend the idea and show what happens when electrons have a mobility comparable to that of holes. When ignoring the sub-threshold ("minority carrier") concentrations, the basic equations are replaced by

$$V(x) > V_g: \quad p(x) = \frac{C_{ox}[V(x) - V_g]}{q} \tag{17}$$

$$n(x) = 0 \tag{18}$$

$$V(x) < V_g: \quad p(x) = 0 \tag{19}$$

$$n(x) = \frac{C_{ox}[V_g - V(x)]}{q} \tag{20}$$

and

$$I_x(x) = qW\left[p(x)\mu_p + n(x)\mu_n\right]\frac{dV(x)}{dx} \tag{21}$$

with μ_p and μ_n the effect field-effect mobility of holes and electrons, respectively. In the general case, the solution is not just treating the device separately as p-channel and n-channel devices and then summing the currents, because both types of charge and current can exist at the same time in different parts of the device (with carrier recombination at the transition point in space). When the gate bias is outside the range 0–V_{ds} it has only one type of charge throughout the device and it can be treated as a p-channel or n-channel device. Care has to be taken when V_{ds} and V_g are not of the same sign. It can be shown, by using device symmetry operations and potential offset invariance, that this, effectively, is equal to subtracting the drain bias from the gate bias and inverting the drain–source potential. As an example, $V_{ds} = 1$ V and $V_g = -5$ V is equal to $V_{ds} = -1$ V and $V_g = -6$ V and the current is totally p-type. A more complicated case exists when the gate bias is in the range between the drain and source potential. In this case, there exists a region of length L_n with free electrons and a region of length L_p with free holes, see Fig. 9. At the junction point, the potential is equal to the gate-bias. When we assume that at this junction the electron–hole recombination is not the limiting factor, we can treat each region as an FET in saturation. Then, demanding equal current in both regions (example for $V_{ds} > 0$):

$$\frac{1}{2}\frac{W}{L_p}C_{ox}\mu_p\left(V_{ds} - V_g\right)^2 = \frac{1}{2}\frac{W}{L_n}C_{ox}\mu_n\left(V_g\right)^2 \tag{22}$$

and knowing that the total length is equal to the channel length:

$$L_p + L_n = L \tag{23}$$

will yield (for $V_{ds} > 0$):

$$I_{ds} = \frac{1}{2}\frac{W}{L}C_{ox}\left[\mu_n V_g^2 + \mu_p\left(V_{ds} - V_g\right)^2\right] \tag{24}$$

In the same way can be found for $V_{ds} < 0$

$$I_{ds} = -\frac{1}{2}\frac{W}{L}C_{ox}\left[\mu_n\left(V_{ds} - V_g\right)^2 + \mu_p V_g^2\right] \tag{25}$$

Fig. 10 shows transfer curves of ambipolar devices. The thick parts of the curves indicate this dual-injection regime. The minimum of a particular transfer curve can be found by taking the

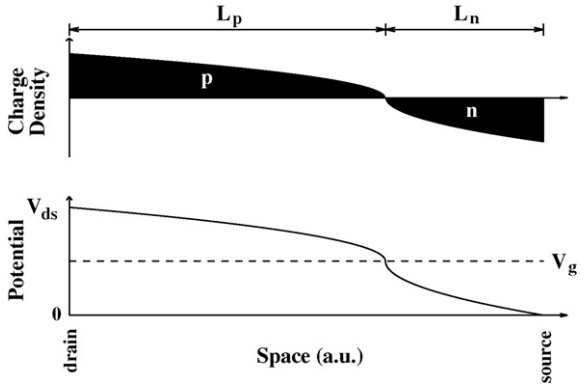

Fig. 9. Charge distribution and potential in an ambipolar TFT when the gate bias is in between the drain and the source bias. For this conditions, the device is in a dual-injection regime, with a zone of positive and zone of negative charge. In this example: $\mu_p = 2\mu_n$, $V_{ds} > 0$ and $V_g = V_{ds}/2$.

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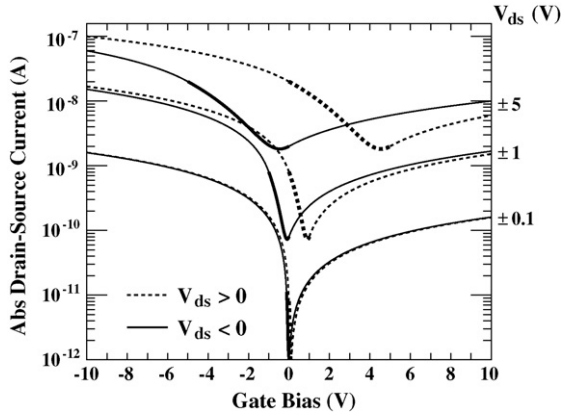

Fig. 10. Transfer functions for ambipolar devices for drain–source biases as indicated. The thick parts of the curves indicate the dual injection regime as shown in Fig. 9. The solid curves are for negative drain–source biases whereas the dashed curves are for positive V_{ds}. Parameters as in Table 1, and $\mu_n = 0.1\mu_p$.

derivative of Eqs. (24) or (25) and putting to zero:

$$V_g^{min}|_{V_{ds}<0} = \frac{\mu_p}{\mu_p + \mu_n} V_{ds} \tag{26}$$

$$V_g^{min}|_{V_{ds}>0} = \frac{\mu_n}{\mu_p + \mu_n} V_{ds} \tag{27}$$

$$I_{ds}^{min} = \frac{1}{2}\frac{W}{L} C_{ox} \frac{\mu_p \mu_n}{\mu_p + \mu_n} V_{ds}^2 \tag{28}$$

The ratio the positions of the minima in positive and negative bias thus directly yields the ratio of electron and hole mobility and can serve as a rapid evaluation tool of the material properties.

Since normal saturation does not exist anymore (no infinitely thin zone can support a finite voltage drop), the effect on the *I–V* curves is pronounced, see Figs. 11 and 12. Note the absence of saturation for $V_{ds} > V_g$. After initially settling on a plateau, as for normal saturation, the current continues to increase rapidly. To highlight the effect, the mobilities were chosen more similar here ($\mu_n = 0.3\mu_p$).

There are many reports in literature about ambipolar TFTs [44,51–55]. At first sight, the curves presented here are slightly

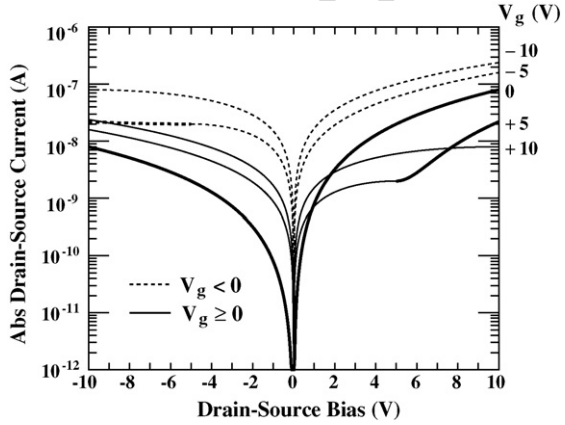

Fig. 11. *I–V* curves in logarithmic scale for ambipolar devices for gate biases as indicated. The thick parts of the curves indicate the dual injection regime as shown in Fig. 9. $\mu_n = 0.1\mu_p$.

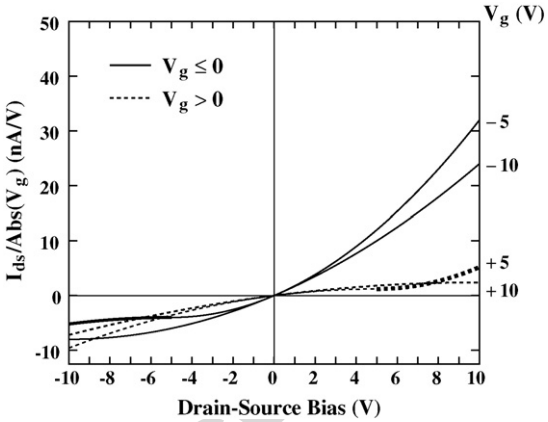

Fig. 12. *I–V* curves in linear scale for ambipolar devices for gate biases as indicated. The thick parts of the curves indicate the dual injection regime as shown in Fig. 9. $\mu_n = 0.3\mu_p$. The curves have been scaled by the gate bias for visibility.

different from curves reported in literature. It has to be born in mind that the simulations assume a zero threshold voltage for both the n-channel and p-channel. In reality this threshold voltage can be substantial and this distorts the curves. In first instance, it will shift the transfer curves of Fig. 10 by the threshold voltage if V_t is equal for hole conduction as electron-conduction. The picture becomes more complicated when they are different. Even worse is the case when the threshold voltage is changing during the measurements, in so-called stressing [56]. This also allows for a separation of the n-channel and p-channel threshold voltages when the stressing is substantial in the time scale of the measurements.

7. Summary and discussion of trap-free TFTs

The model presented here is based on a single postulate, namely rigorously maintaining the linear charge–voltage relation of Eq. (1). As examples of things that are not included are diffusion currents, band-bendings and flat-band voltages. For inversion-channel MOS-FETs these are essential to explain the electrical characteristics. As we have shown, for thin-film FETs they are not needed. In spite of the simplicity of the model, it manages to explain the basic electrical characteristics of TFTs very well. To justify the simplicity of the model we use Occam's Razor; everything that is not essential in a model to explain the data has to be removed to come up with the best model.

The major question is then: what are the essential ingredients for a transistor? Why do some materials result in good transistors and others not? Analyzing the model, it can be said that the only thing that is needed is that the active layer is made of a semiconductor material with a high charge carrier mobility. When a transistor based on a certain material does not show good transistor behavior, it is probably due to low mobility, for instance because it is limited by the presence of a huge amount of traps (as shown in the second part of the document).

Moreover, there are no restrictions as to the dimensions of the device. In the MOS-FET model a device has a minimum size, both in the direction of the current, because the contacts are

pn-junctions, as well as in the direction perpendicular to current because extended band-bendings are needed to induce a channel. A TFT does not need band-bendings, neither at the contacts, nor to induce a channel. It is therefore foreseen that a TFT can be made from three molecules. One very conductive molecule serves as metal and another has a LUMO–HOMO separation which would qualify it as a semiconductor and serves as active material that accommodates the channel. These two molecules need then be separated by vacuum or any material with high band-gap, making it an insulator. The lower limit for the scale of such a device is then determined by the state of technology of molecular engineering.

The similarity of the basic equation, Eq. (3), and the shapes of the curves of Fig. 2, with those obtained for inversion-channel MOS-FETs [10], might explain the persistence in literature of using the MOS-FET model to describe TFTs; empirically, the curves are the same. The complications start when the measured data are analyzed and parameter extraction is attempted. As a good example may serve the determination of the donor density from the threshold voltage, something that is common for a p-type inversion-channel MOS-FET, but does not make sense in the TFT framework, since the doping concentration is not a parameter in accumulation TFTs.

The effects of the contacts were discussed. In literature, contact effects are often mentioned as a source for non-linearities. Here we showed that neither contact resistance, nor contact Schottky barriers can explain non-linear *I–V* curves (for TFTs as well as MOS-FETs). Then, the metal contacts were analyzed in more detail for TFTs. The conclusion was here that these can cause a (tiny) threshold voltage. More important, it shows that the channel can have a potential, even in the case of zero bias. This is relevant in view of the experimental observation of such a voltage drop [49].

Finally, ambipolar devices were discussed. The type of ambipolar device discussed is one in which in the same material for both holes and electrons the mobility is high enough to allow for an appreciable current. There exist other technological solutions of making ambipolar devices, such as hetero-devices, with an electron-transport layer on top of a hole-transport layer, or vice versa, but such devices are not studied here. The material itself is assumed to be intrinsically ambipolar.

Diffusion currents are not considered in the model. There is a fundamental reason for that which becomes clear when we compare it to the MOS-FET model. For an MOS-FET, below threshold, the charge density is exponentially depending on the voltage [10]. Since, in the linear region, the voltage is slightly higher at one electrode compared to the other, the density is exponentially larger there. Hence, a large density gradient exists in the channel below threshold. In a TFT, however, the densities depend linearly on the local voltage and no large density gradients can exist. Therefore, in a TFT, the drift currents, which depend on the density and not on the gradient, always dominate and the diffusion current is practically zero.

In the second part we will show that we have to extend the model to describe things like field-dependent, bias-dependent and temperature-dependent mobility as well as the transient behavior.

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