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ScienceDirect
Organic Electronics 8 (2007) 300–304
Organic Electronics
www.elsevier.com/locate/orgel

Metal contacts in thin-film transistors

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Received 9 December 2005; received in revised form 24 July 2006; accepted 29 November 2006
Available online 22 December 2006

Abstract

The effects of metal contacts on the electrical characteristics in thin-film transistors are discussed. It is found that the effects of these contacts are twofold. First, a constant potential that can range from zero to some volts (half the bandgap) is added to the entire channel. Second, a residual barrier is formed with a height that depends on the bias, and is in the order of tens of meV when a current is present. It is shown that these predicted effects are in agreement with experimental observations.

PACS: 85.30.De; 85.30.Tv

Keywords: Thin film field-effect transistors; Amorphous silicon; Organic semiconductors; Two-dimensional electronics; Contact effects

Thin film field-effect transistors (TFTs) are made from the deposition of a thin active layer on top of an insulator. Because of the flexibility in design – the insulator and active layer do not have to be necessarily of the same material – they have taken a tremendous leap in recent years. Most commonly made from (amorphous) silicon on silicon oxide [1], with applications in active matrix displays, modern devices also include organic materials. Such materials can be made flexible as well as transparent or emitting light in the full range of colors. Together with the low cost of production, this extended the number of possible applications; unique devices are possible [2–4].

Thin-film transistors (TFTs) are transistors in which the active current-carrying layer is a thin film, in contrast to MOS-FET transistors where the currents are in the bulk of the material. The use of organic materials allows for a fabrication of the devices by printing techniques, thereby largely reducing the cost. Disadvantages of TFTs are a lower quality (crystallinity) of the active layer resulting in a lower mobility of charge carriers and therefore lower switching speeds. For this reason, TFTs find main applications in which the switching speed is not crucial, for instance in active matrix displays. Future applications also include flexible electronics, an area only feasible with (organic) TFTs. From bottom to top, a typical TFT consists of (1) a substrate giving support to the device, (2) a metal, or highly doped semiconductor taking the role of the gate electrode, (3) an insulator separating the gate from the active layer (4) metallic contacts serving as drain and source electrodes for injection and collecting of charges, and (5) the active semiconductor

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1566-1199/$ - see front matter
doi:10.1016/j.orgel.2006.11.004

layer. In some TFT geometries, the source–drain electrodes are deposited on top of the active layer, both geometries having their pros and cons. Finally, some TFTs have an additional capping layer to protect the device from external influences (diffusion of impurities, such as water, etc.). While originally made from CdS and CdSe, the most widely used and best studied devices are TFTs of (amorphous) silicon on silicon oxide [1].

One of the problems encountered in TFTs is the way to describe the effects of the metallic contacts. TFTs are normally described in the framework of the metal-oxide-semiconductor field-effect transistor (MOS-FET) model [5]. It is then common to attribute all deviations from MOS-FET behavior to the effects of the contacts, sometimes also generically termed contact resistance, although the effects include much more than simple ohmic resistance. Contact effects are well studied in the MOS-FET model and a multitude of reports exist to describe them, see for example the summary of Vega [6]. Some attempts exist to extend the theory to TFTs as well, see for example Necliudov et al. [7] and Hamadani and Natelson [8].

To compare, in a standard MOS-FET the contacts are made from the same material as the channel, but with a different doping type. Once an inversion channel of free charge is induced, the conduction and valence bands have aligned across the device from source to drain and no energetic barriers exists for the injection of carriers into the channel. Modern thin-film transistors, even when made from (amorphous) silicon, often have metallic contacts. Thus, when a channel is induced a barrier might still exist.

The active layer in a TFT is best treated as two-dimensional. This is applicable to thin-film transistors and thick FETs when in accumulation (when the charge in the channel is of the same type as the majority carriers in bulk material). The latter is true because, in the absence of electronic states to store immobile charge of the correct sign, all induced charge is mobile charge and therefore necessarily close to the interface since there is nothing opposing the pulling force of the electric field. To give an idea of how thick a channel in a MOS-FET is when in accumulation, or what the minimum thickness for the active layer in a TFT is and still function properly. For a device, with an oxide (insulator) thickness of 200 nm, operating at 1 V gate bias (with drain and source grounded), the induced charge density in the channel is $0.17\,\mathrm{mC/m^2}$. Assuming that the active layer is made of silicon with an effective density of valence band states of $N_V = 1.06 \times 10^{19}\,\mathrm{cm^{-3}}$ [9], the induced charge can easily fit in a monatomic layer. This explains why the measured mobility in TFTs is normally found to be independent of layer thickness after the first monolayer [10,11] and why the first layer and the interface with the insulator plays a key role in the device properties. As a result, we can imagine all densities of charge and states as true two-dimensional entities, without loss of accuracy [12].

In the current work, we describe the metallic TFT contacts when the device is in accumulation. We describe a p-channel accumulation device, but with the appropriate changes it is equally applicable to n-channel accumulation devices. As an immediate observation it can be stated that, when the device is working in accumulation, there are no depletion zones at the contacts and they can therefore not be treated as Schottky barriers, as is common for metallic contacts in MOS-FETs.

Fig. 1 shows a cross section of a TFT with the definitions used in the current work. As mentioned above, we consider the active layer as truly two-dimensional, where, at any point x along the channel, the local charge density $\rho(x)$ is directly linked to the local potential $V(x)$:

$$\rho(x) = C_{ox}[V(x) - V_g], \tag{1}$$

with C_{ox} the insulator capacitance density and V_g the bias at the gate. The implications of rigorously maintaining this relation will now be demonstrated.

Fig. 2 shows a schematic energy diagram of an unbiased metal–semiconductor–metal system. Because of the difference in Fermi level, E_{Fm} in the metal and E_{Fs} in the semiconductor (with ΔE_F defined as the difference), the system can gain energy by transferring electrons, in the case of Fig. 2 from semiconductor to metal (or holes from metal to semiconductor). The conventional buildup of space charge by uncompensated ionized acceptors or donors via Poisson's equation as in Schottky barriers does not take place due to the non-existence of

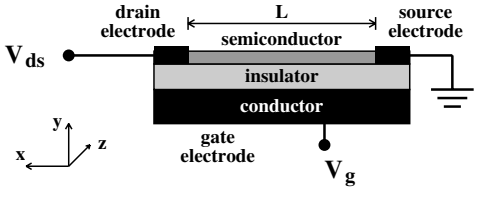

Fig. 1. Cross section of a thin-film FET (TFT) with the definitions used in the current work.

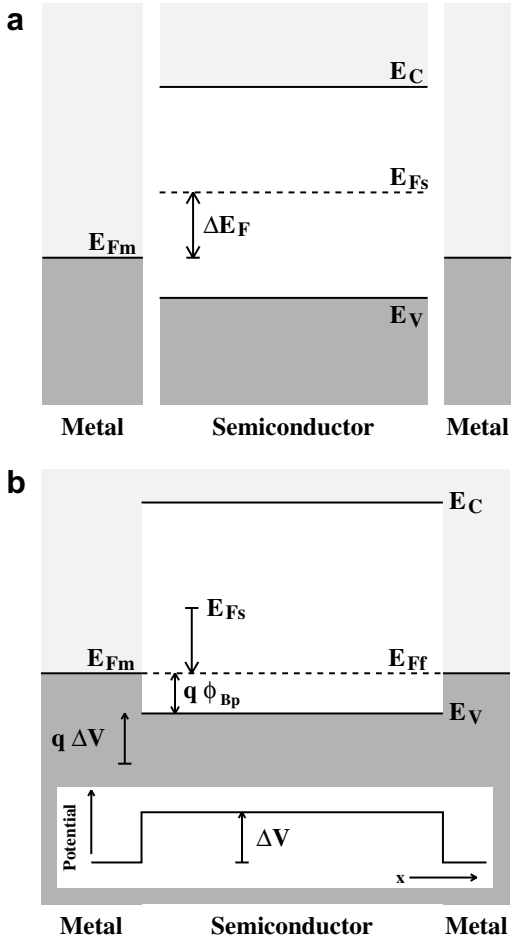

Fig. 2. Schematic energy diagram of a metal-contact TFT before (a) and after (b) contact. The parameters are: E_{Fm}, Fermi level in the metal; E_{Fs}, Fermi level in semiconductor before contact; E_{Ff}, Fermi level in semiconductor after contact; E_{C} and E_{V}, conduction band and valence band respectively; ΔV, voltage drop at the interface and equal to the voltage in the channel, as shown in the inset.

such impurities ionizable with the correct sign. Instead, the charge flowing into the channel is solely comprised of free holes. As a first effect, the holes cause a change of the Fermi level from E_{Fs} to E_{Ff} according to the Boltzmann relation:

$$p = N_{\mathrm{V}} \exp[(E_{\mathrm{V}} - E_{\mathrm{Ff}})/kT], \tag{2}$$

with N_{V} the effective (two-dimensional) density of valence band states, E_{V} the energy of an electron in the valence band, k Boltzmann's constant, T the absolute temperature and E_{Ff} the final position of the Fermi level. As a second effect, the new free holes are adding a potential to the channel (and to all energy levels in the channel) via Eq. (1),

$$\Delta V = qp/C_{\mathrm{ox}}, \tag{3}$$

with q the elementary charge. The free-hole density and thus the potential are constant over the entire length of the channel, because any gradient in either will cause a redistribution of the charges until the gradients disappear. At steady state, the only solution is a homogeneous distribution of holes and a constant voltage in the channel. The two effects, changing the Fermi level and increasing the in-channel potential, continue, until the Fermi levels have lined up, $E_{\mathrm{Ff}} = E_{\mathrm{Fm}}$. Combining the above two equations, with the definition of ΔE_{F}, the potential in the channel will be given by

$$\Delta V = \frac{kT}{q} W\left(\frac{q}{kT} A\right), \tag{4}$$

with W the Lambert-W function, and A equal to

$$A = \frac{qN_{\mathrm{V}}}{C_{\mathrm{ox}}} \exp\left(\frac{E_{\mathrm{V}} - E_{\mathrm{Fm}}}{kT}\right). \tag{5}$$

At the same time, a residual barrier $q\phi_{\mathrm{Bp}}$, equal to the difference in Fermi level and valence band in the semiconductor, exists at the contacts. Combination of Eqs. (1) and (2) yields,

$$q\phi_{\mathrm{Bp}} = -kT \ln\left(\frac{C_{\mathrm{ox}}(\Delta V - V_{\mathrm{g}})}{qN_{\mathrm{V}}}\right) \tag{6}$$

This barrier height thus depends on the bias V_{g}. When the bias is changed, the density of free holes changes and the Fermi level depth changes and the barrier height with it.

The easiest way to measure the height of the barrier is via the temperature dependence of the drain–source current. However, this necessitates the existence of a channel and thus free holes. Free holes imply that the Fermi level in the active layer is close to the band edge. The Fermi level depth being equal to the barrier height (see Fig. 2) then tells us that the measured barrier height is always rather small, in the order of tens of meV. We can thus give an estimate for the measured barrier height by substituting typical values for the parameters: $N_{\mathrm{V}} = 1.06 \times 10^{16}\ \mathrm{m}^{-2}$, $C_{\mathrm{ox}} = 170\ \mu\mathrm{F/m}^2$, $V_{\mathrm{g}} = -1$ V and $T = 300$ K yields about 60 meV for the barrier height. For the same reason, the barrier height, when measured by current, is independent of the type of metal used for the contact, since it depends only on the final Fermi level depth; at most, a slightly different threshold voltage results.

An observation can also be made for the in-channel potential ΔV. It can take values ranging from

zero up to the volts range. For intrinsic materials, even a tiny amount of charge in the channel can shift the Fermi level substantially and it is thus possible that the effect is nearly completely absorbed by a shift of the Fermi level, $E_{Fs} - E_{Ff} \approx \Delta E_F$, and $\Delta V \approx 0$. On the other hand, in a system where the Fermi level is pinned, for instance in doped semiconductors, the effect is mainly a voltage drop at the contact, $\Delta V \approx \Delta E_F/q$ and this can easily be in the volts range.

Summarizing, the metal contacts of a TFT working in accumulation cause two effects: (i) the building up of an in-channel potential that can be in the volts range and (ii) the formation of a residual barrier, with a height that depends on the gate bias and, when measured, is of the order of some tens of meV.

Relevant in view of this, are the experimental results reported in literature. Yagi et al. report on a gate-bias-dependent barrier with, for a certain bias, an activation energy of 80 meV [13] which is very close and easily within the range of the prediction above. Note that the devices of Yagi have top electrodes, a slightly different geometry compared to the bottom electrode devices presumed here. Apparently, the difference between the two geometries is not important enough and the model still applicable.

Concerning the in-channel potential predicted above, relevant is the voltage profiling experiment of Bürgi et al. [14]. They measured a potential in the channel, in the absence of bias, with an order of magnitude as described in the current work. Others report similar Kelvin probe experiments, but without presenting the most relevant zero-bias results.

Some observations have to be made about the limitations of the model. First of all, in Eq. (2), the Boltzmann approximation to the full Fermi-Dirac distribution has been used. This simplification is done to make the idea more understandable and make it analytically solvable. For Fermi levels close to – or resonant with – the valence band, this approximation is no longer valid. Note however that for such systems, the barrier height goes to zero and the effects of the contacts disappear completely.

Moreover, even a negative barrier height is predicted for large biases. The model thus loses applicability for such conditions. What happens for large biases is that all available states N_V are occupied by holes and saturation is thus expected for the transfer curves. As long as such saturation is not observed, the model is apparently applicable. In practice what will happen is that when the states in the first monolayer are depleted, the second layer (if present) starts getting filled. This layer is slightly more distant from the gate electrode and feels a slightly different capacitance and a different charge–voltage relation exists, compared to Eq. (1). To a good approximation, when the insulator is much thicker than a monolayer, it can be imagined that the DOS is simply multiplied by a factor 2 and then 3, etc. The simplified model presented only describes non-degenerate cases for low biases. Moreover, in practice it is expected that burning through the oxide occurs long before depletion of the valence band sets in, especially for thicker devices.

It was stated that no band bendings occur at the contacts. This is not entirely true. Band bendings can occur, but the spatial extent is rather small. To give an idea, were a classical Schottky barrier analysis used [9], with a density of states of $N_V = 10^{19}\,\mathrm{cm}^{-3}$, and a voltage drop at the contacts of $V_{bi} = 1$ V, this gives a space charge region of 8 nm. (Note that the value of N_V was used instead of N_D because the space charge is caused by free holes rather than ionized donors). In this regime, the tunneling will dominate over thermionic emission and the band bending region does not impede carrier injection. In fact, this strategy is normally followed to make ohmic contacts, where inter-diffusion of material at the interface is stimulated so as to allow for a high density of space charge and a small band bending region.

In summary, we have shown here, based on a single assumption of treating the active layer of thin-film transistor as a two-dimensional entity, the effects of the contacts. The idea is that if a current is present, however tiny, as long as it is observable, there must be free charge in the channel and consequently, the Fermi level must be somewhere close to the states responsible for conduction (for simplicity, these states are considered band states). Because on the other side the Fermi level is equal to the top of the Fermi sea, the barrier is rather small and injection to these conduction states are never a limiting process.

This work is relevant because it applies to all TFTs with any combination of active layer and contact metal, as long as the transistor is working in accumulation and band bendings are either absent or limited in size. Finally, it has to be pointed out that the theory described is for pure metal–semicon-

ductor–metal structures, with homogeneous materials and abrupt interfaces. Any diffusion or reaction taking place at the interface can undermine the validity. In fact, the current level of technology of organic TFTs makes most of them probably of a non-ideal type. Moreover, the workfunction of the metal can cause the semiconductor to go into depletion instead as the above described accumulation, in which case a threshold voltage is expected to exist, turning the device into a normally-off FET. Only after overcoming this threshold voltage does the theory apply.

Acknowledgement

This work has been financed by Portuguese grant POCTI/FAT/47956/2002 and POSC research unit CEOT.

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