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Interface state mapping in a Schottky barrier of the organic semiconductor terrylene

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Abstract

In this work we quantitatively map interface states in energy in a Schottky barrier between aluminum and the vacuum sublimed organic semiconductor terrylene. The density map of these interface states was extracted from the admittance spectroscopy data. They revealed an interface state density of $\approx 2 \times 10^{12}$ cm^{-2} eV^{-1} close to the valence band which decreases slightly towards midgap. Additional dc measurements show that the semiconductor bulk activation energy is 0.33 eV which may correspond to an acceptor level.

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Keywords: Organic semiconductors; Interface states; Schottky barrier

1. Introduction

Conjugated organic materials have a wide application in thin-film electronics. One of the main advantage is the fact that they can be produced in large quantities by simple techniques such as spin coating which lowers the production cost dramatically. On the other hand, we know from the classical semiconductors that device production at ambient conditions limits the control over the interface, specifically the electronic states at the junctions of two materials. These interface states can help, for example by aligning the energy bands of the two materials, thereby facilitating carrier injection, but in most cases, the interface states have detrimental effects on the device by causing an unwanted change of the bandstructure and blocking possible conduction paths and lowering the device performance. In any case, it is important to quantify them. See the book of Sze for an overview of the effects of interface states [1].

The importance of interfaces on device performance has also quickly become apparent for organic-based semiconductors; many groups have done research to specifically address this issue [2–6]. As an example, it is now well accepted that reactive metals such as calcium and aluminum interact chemically with the polymers and lead to new chemical species [7] which in turn deeply affect its electronic structure and, hence, the electronic process taking place at the interface.

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Thus, in stead of the sharp boundary between metal and semiconductor, as presented in most semiconductor textbooks, the interface in general contains a reacted region with new dielectric properties. We think such a region exists in our devices and it behaves as a thin, insulating interfacial layer (20–40 Å thick). The resulting device can be treated as an MIS (metal–insulator–semiconductor) tunnel diode. Furthermore, because, as we will show, the currents through the diodes are so small (as to not significantly disturb the equilibrium condition) we can observe signals from the interface states.

The simplest and most widely applied technique to characterize interface states in MOS structures is admittance spectroscopy. This technique was developed by Nicollian and Goetzberger in the early days of semiconductor science [8]. The imaginary part of the admittance, i.e., the capacitance, is directly related to the charge trapped and released from the interface states as a consequence of time varying excitation, the external ac voltage. Stationary occupancy is manipulated by varying the (dc) bias and, therefore, the band bending associated with the Schottky barrier. With this technique, spatial and energetic distribution of states within the space charge region can be probed by varying the frequency, temperature, and bias.

In this contribution we use the admittance technique to estimate the density and energetic distribution of states at the interface of a conjugated oligomer and aluminum. The conjugated material is terrylene, a three-unit oligomer of poly(peri-naphthalene) (PPN). This material has an interesting molecular structure, intermediate between polyacetylene and graphite. The resulting rigid, planar structure (see Fig. 1) has large overlap of the orbitals with neighboring molecules and the material is therefore expected to have excellent structural stability and high carrier mobility. In another publication we will present our mobility measurements on FET devices. Here we focus on the interface states as measured in Schottky barriers.

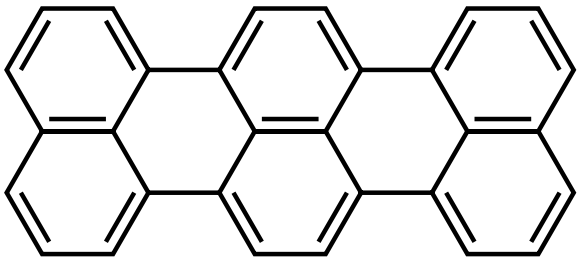

Fig. 1. Molecular structure of terrylene. The resulting planar form is expected to increase the mobility of the carriers and to cause high structural stability.

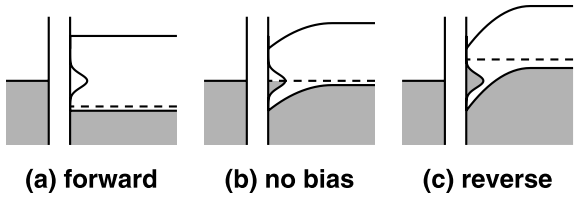

Fig. 2. Example of a bunch of interface states and their change of occupancy upon changes of bias. The three pictures show a device made of a metal (left), a thin insulating layer and a semiconductor (right) for different biases. The dashed line indicates the Fermi level and the interface states are schematically represented by a bell-shaped curve next to the insulator.

2. Theory

As mentioned above, the structure that we are measuring is a Schottky barrier with a thin insulating layer between the metal and the semiconductor (Fig. 2). The insulating layer disconnects the interface states from the metal, making them communicate with the semiconductor more readily than with the metal. The insulating layer lowers the background current and facilitates the observation of the signal signatures arising from these states. Our analysis is based on the works of Nicollian and Goetzberger [8] which have later been extended by a variety of people such as Kar and Dahlke [9,10], Deneuville [11], Vicent et al. [12], Sapega [13], and Barret and Vapaille [14,15]. See also the summary of effects of interface states in [1].

The first step is to determine the effect of interface states on the admittance. An ac signal, superimposed on a dc bias will cause the Fermi level to oscillate around a mean position. Any interface states within the modulation depth v_{ac} around this average Fermi level will change their occupancy during an ac cycle and the emitted and captured charges contribute to a capacitance,

$$C_{is} = \Delta Q/\Delta V = Aq^2 N_{is}, \tag{1}$$

with A the area of the device, q the elementary charge and N_{is} the density of interface states per eV per unit area. The charges come out with a characteristic time constant τ. For low frequencies compared to this time constant, the measured capacitance is as given by Eq. (1). For increased ac frequencies ω, the response of the states to the signal is diminished; the reduced ac current means a reduced measured capacitance. The slower response also causes a phase lag of the ac current and the capacitance can be measured as a conductance and loss, G and G/ω, respectively. Standard procedure is to model this with an equivalent circuit of a capacitance in series with a resistance [16], see Fig. 3, in which the capacitance is equal to C_{is} and the resistance is such that the time constant RC of this circuit is equal to the relaxation time τ of the levels. Note that whereas the capacitance has real physical meaning in this circuit, the resistance only helps to define the time constant. To find the *measured* capacitance and loss (C_p and G_p/ω respectively) of this circuit and

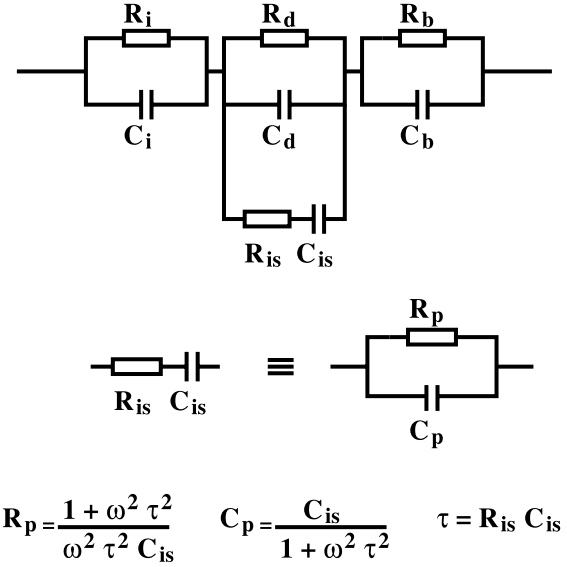

Fig. 3. Equivalent circuit (top) used to describe the measurements. The subscripts 'i', 'd', 'b' and 'is' denote the interface layer, the depletion region, the bulk zone and the interface states, respectively. The bottom part shows how to convert the serial sub-circuit of the interface states into a parallel circuit.

hence of the interface states, we have to translate the serial circuit of C_{is} and R_{is} into a parallel circuit,

$$C_p = \frac{C_{is}}{1+\omega^2\tau^2}, \tag{2}$$

$$\frac{G_p}{\omega} = \frac{\omega\tau C_{is}}{1+\omega^2\tau^2}, \tag{3}$$

with $\tau = C_{is}R_{is}$. The maximum in loss occurs at $\omega = 1/\tau$ and is exactly half the low-frequency capacitance,

$$(G_p/\omega)_{max} = Aq^2 N_{is}/2, \tag{4}$$

$$\omega_{max} = 1/\tau. \tag{5}$$

In this way, by measuring the capacitance C_p and loss G_p/ω as a function of frequency, the density of states at a region $qv_{ac} + kT$ around the Fermi level can be determined. By reducing the ac modulation depth (nominally 50 mV) the number of states contributing to the admittance can be reduced and the resolution of the measurements increased, at the expense of less signal. The resolution can also be improved by lowering the temperature (at room temperature $kT = 26$ meV) at the expense of unpractical low modulation frequencies.

The second part of the mapping is the determination of energetic position of the states for which we have just found the density. This can be found by determining the movement of the peak in loss with temperature. The trap relaxation time τ follows [17]

$$\tau = \tau_0 T^{-2} \exp\left(\frac{E_T - E_V}{kT}\right), \tag{6}$$

with τ_0 still depending on the density of states at the top of the valence band, the average thermal velocity of the carriers and the capture cross section, but not depending on the temperature. Combining Eqs. (5) and (6) learns us that an Arrhenius plot of the maximum in the loss as a function of temperature will yield the activation energy, $E_A = E_T - E_V$, of that particular bunch of states,

$$\omega_{\max}(T) = \omega^0_{\max} T^2 \exp(-E_A/kT). \quad (7)$$

To find the distribution of interface states in energy we can scan the bias and repeat the above procedure at every step. For every bias the band bending will be different and the Fermi level will cross another bunch of states at the interface. As an example, for forward biases the band bending is decreased and the Fermi level will be closer to the valence band at the interface. We therefore expect to probe shallower, faster states, and the maximum in loss should shift to higher frequencies. Note that this is fundamentally different than the situation of discreet deep levels homogeneously distributed in space. In that case, the Fermi level will cross the deep level at a different position in space (closer to the interface), but at the same place in energy relative to the valence band and the relaxation from the levels is therefore invariant under a change of bias and we do not expect the peak in loss to shift with bias for discreet levels.

When applying the above model to organic Schottky barriers, we have to bear in mind that the diode is made up of a depletion region, a bulk region and a thin interfacial layer, placed in series. Each has its own conductance and capacitance. The interface states are then in parallel with the depletion region, see Fig. 3 for the complete equivalent circuit. The measured capacitance and conductance can, therefore, not simply be assumed to arise solely from the interface states. However, it is easy to show that when the device cut-off frequency determined by the RC networks of the bulk and depletion layers is beyond the natural frequency $\omega_{\max}$ of the interface states, the position and amplitude of the peak in loss caused by the interface states is unaffected by these loops and Eqs. (4) and (5) still hold. In our measurements, this cut-off frequency was always above $\omega_{\max}$.

Finally, some authors use more elaborate models for describing Schottky barrier devices with interface states. Wu and Yang attribute the diode capacitance to a modulation of the effective Schottky barrier height by interface charges [18]. The charges at the interface contribute to the space charge and depletion width in the depletion region. Werner et al. use a similar model to describe a Schottky barrier where the contribution of interface states to the admittance is indirect rather than direct as described above [19]. In this work we analyze the data in a more classical way, although we are well aware of the limitations of and possible improvements to the model.

3. Experimental

Fig. 4 shows the Schottky barrier diode structure used for the current study. It consists of a gold/terrylene/aluminum sandwich device deposited on top of silicon. Note that the silicon plays no part in the device and is only used as a well defined, flat substrate. The gold–terrylene interface is an ohmic contact and we do not expect any rectifying properties from it. The aluminum–terrylene interface on the other hand forms a rectifying Schottky barrier which forms the object of the current study. The terrylene has been deposited by sublimation under high vacuum conditions (10^{-6} mbar). In order to keep the deposition rate constant (1–1.5 nm/min) the sublimation temperature was increased during the film preparation from 250 up to 315 °C. The reason of this behavior is yet under study but is related to the tendency of terrylene to form clusters inside the cell and is strictly depending on the evaporation rate, being less evident with faster rates. The final thickness of the organic layer is in the order of 65 nm. Before depositing the terrylene, a thin gold layer (30 nm) was deposited on top of the silicon substrate via thermo-joule evaporation and in the same way the circular aluminum electrodes with a diameter of 1.5 mm were deposited through a mask on top of

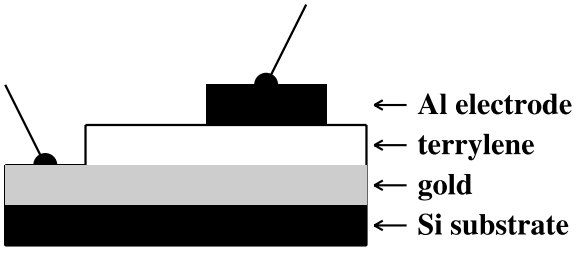

Fig. 4. Device structure (not to scale) used in the current study. For forward bias the gold electrode is at higher bias with respect to the aluminum electrode.

the terrylene. The measurements were done in low vacuum (10^{-3} mbar) at room temperatures or high vacuum (10^{-6} mbar) at other temperatures.

4. Results

Fig. 5 shows a typical *IV* curve of a Schottky barrier as shown in Fig. 4. Apart from the low rectification ratio, the figure shows that the material is a poor conductor with currents below 10^{-8} A/cm^2 in the entire range shown (-2 to 2 V). Such low conductivity indicates a small number of free carriers and we can expect the thin film to be completely depleted in equilibrium (in the absence of bias). Free-carrier concentrations can normally be measured in capacitance–voltage measurements. As can be seen in the Mott–Schottky plot ($1/C^2$ versus V) of Fig. 6, the capacitance is independent of voltage for reverse and small-forward biases. This indicates that at these voltages the sample is fully depleted, in line with the *IV* measurements, and it is not possible to determine the free-carrier density here. For forward bias the depletion layer shrinks and does no longer fill the entire thickness of the sample. The slope of the plot at these biases indicates an acceptor density (N_A) of some 10^{16} cm^{-3} and the intersect of the slope with the voltage-axis reveals a built-in voltage (V_{bi}) of about 1 V. On basis of these values we can estimate the thickness of the depletion region

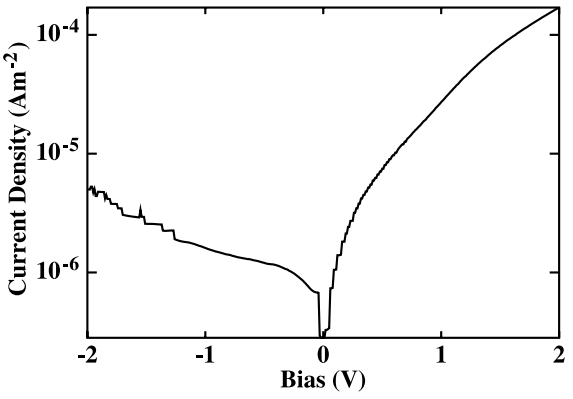

Fig. 5. Typical *IV* curve showing poor conductance and small rectification ratios.

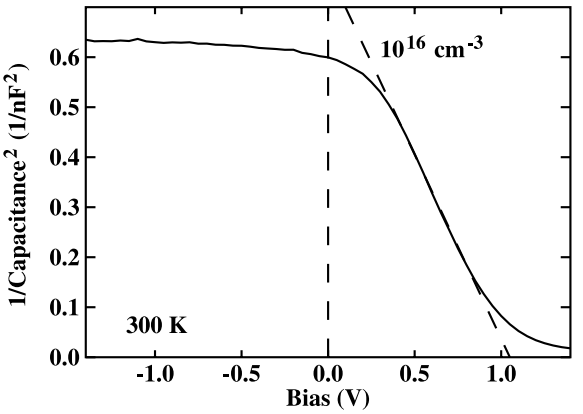

Fig. 6. Typical *CV* plot taken at room temperature and a probing frequency of 100 Hz. The flat region at reverse biases shows that the sample is fully depleted. For forward biases the slope indicates a free carrier concentration of some 10^{16} cm^{-3}.

needed to compensate for the built-in voltage in the absence of external bias. For this we use Poisson's equation,

$$\int\int_0^W qN_A/\epsilon \, dx^2 = V_{bi}, \tag{8}$$

with x space, W the depletion width, ϵ the permittivity (for which we chose $5\epsilon_0$). The result is $W = 110$ nm, indeed larger than our measured sample thickness (65 nm) and the layer is therefore completely depleted. One thing to remark is that the value of the acceptor density, N_A, was derived from the forward-bias data. This is unconventional and as such the values obtained should be used as indicative, rather than absolute.

The bulk activation energy E_{ba} can be measured by putting the device in strong forward bias and measuring the current as a function of temperature.

This current should follow the relation

$$I = I_0 \exp(-E_{ba}/kT), \tag{9}$$

with I_0 not depending on temperature when a small temperature range is scanned. Fig. 7 shows that for a bias of +2 V the bulk activation energy is measured as $E_{ba} = 0.33$ eV. Very similar to the activation energy found in the FET devices (as will be presented in another paper).

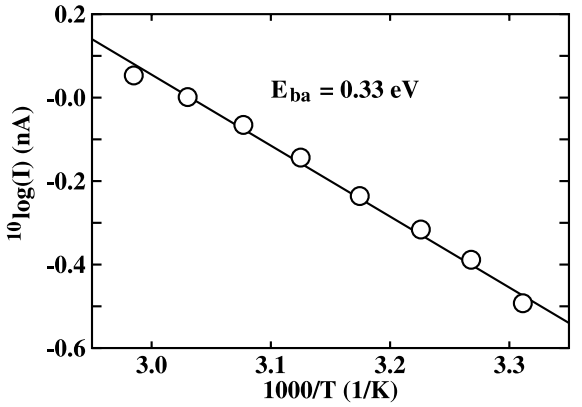

Fig. 7. Dependence of the forward-bias dc current on temperature. The line is a fit with an activation energy of 0.33 eV.

For the remainder of the study, another device was used. The *IV* characteristics of this device were measured at elevated temperatures (see Fig. 8). This temperature, 360 K, is the onset of undoping the device. Beyond this temperature the current drops irreversible and the conductivity becomes even lower. In the figure we can see the first evidence for interface states. The forward-bias current deviates slightly from the standard models that predict an exponential growth of the current (represented by the dashed line in this logarithmic plot). A surplus current around 1 V forward bias is visible. Note that these voltages are still below the bias needed to overcome the built-in voltage and enter the bulk-limited-current regime. The increase in current we assign to an extra path that is opened for the carriers when the Fermi level ligns up with the interface states. In this way, the current via these states is only visible for certain voltages, namely when the Fermi level is resonant with the interface states. The observation of this current is enabled by the extremely low background currents through the device.

Clear evidence for interface states is obtained from the admittance data. Fig. 9 shows the loss as a function of bias. At the same biases where the dc current showed an increased current, the loss shows a peak. This peak moves to higher forward biases when the frequency is raised and eventually disappears when the states stop responding to the probing frequency. The figure shows the loss for 50 and 100 Hz.

We can plot the same admittance data in another form. Instead of showing the loss versus bias with the frequency as a parameter we can also plot the loss or loss tangent ($\tan\delta = G/(\omega C)$) versus frequency with bias as a parameter. This is shown in Figs. 10 and 11. It shows here that we have a peak around 1 kHz, which moves with changes of the bias. For higher forward bias the peak moves to higher frequencies. The fact that the position of the peak moves with changes in bias is expected for interface states and not for discreet levels, as explained in Section 2. We also would like to point

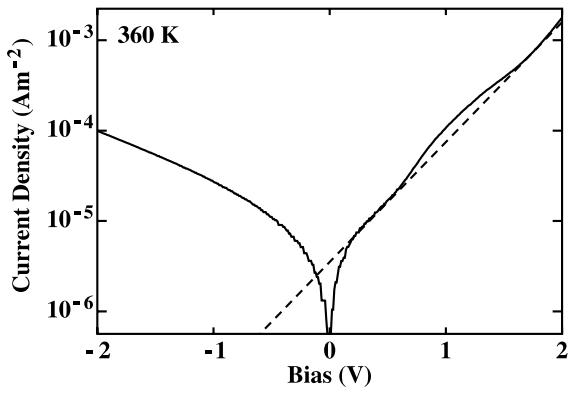

Fig. 8. An *IV* plot of a device at 360 K. The dashed line helps to visualize the deviation from standard diode characteristics in forward bias. This deviation is due to interface states.

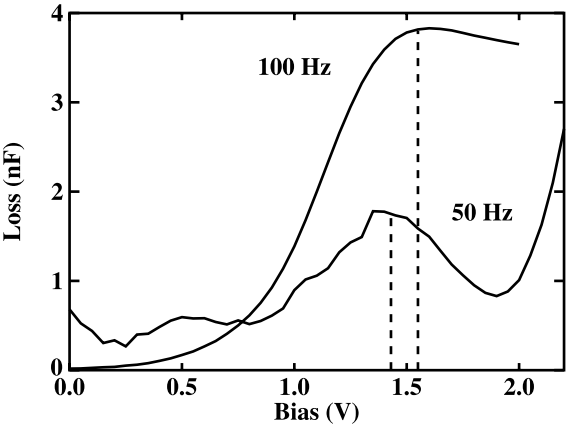

Fig. 9. Loss (G/ω) versus bias for ac probing frequencies of 50 Hz (bottom trace) and 100 Hz (top trace). The peak around 1.5 V is due to interface states.

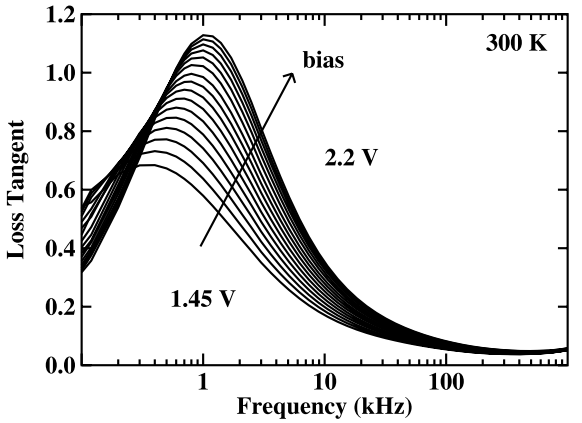

Fig. 10. Loss tangent ($1/\omega RC$) versus frequency for dc biases ranging from 1.45 V (leftmost plot) to 2.2 V (rightmost plot) in 50 mV steps. For stronger biases the Fermi level moves down at the interface and shallower, faster traps are probed. This moves the peak to higher frequencies.

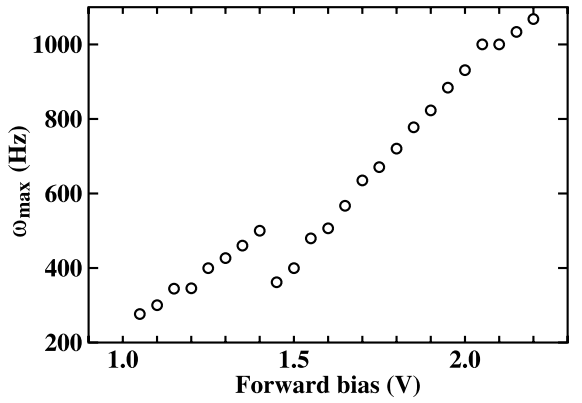

Fig. 11. Maximum of the peak in Fig. 10 as a function of bias for two different runs.

out that a model consisting of only the bulk and depletion regions, without the interface states, cannot adequately describe the data. Such a model predicts the observation of a peak in the loss tangent, but for increased forward bias the bulk region and hence its resistance would increase slightly and the position of the peak should therefore move to slightly lower frequencies in contrast to our observations.

An estimate for the activation energy for these particular states visible at 1.5 V forward bias can be obtained from the temperature dependence of the peak of the loss tangent, see Eq. (7). For the states visible at 1.5 V forward bias this is done in the temperature range 318–362 K and the result is shown in Figs. 12 and 13; a fit to the data yields $E_a = 0.45$ eV. As said before, this is the average activation energy of a narrow band of states, about 50 meV wide.

From Eq. (4) and $(G/\omega)_{max} = 3$ nF and $A = 1.77 \times 10^{-2}$ cm^2 we find a density of interface states of $N_{is} = 1.0 \times 10^{12}$ cm^{-2} eV^{-1} at this energy.

To find the activation energy of states visible at other biases we assume that the Fermi level moves

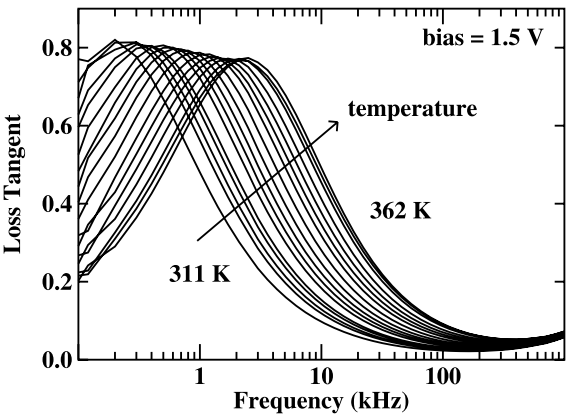

Fig. 12. Temperature dependence of the loss tangent. The peak moves to higher frequencies indicating that the (same) interface states respond faster, according to Eq. (6).

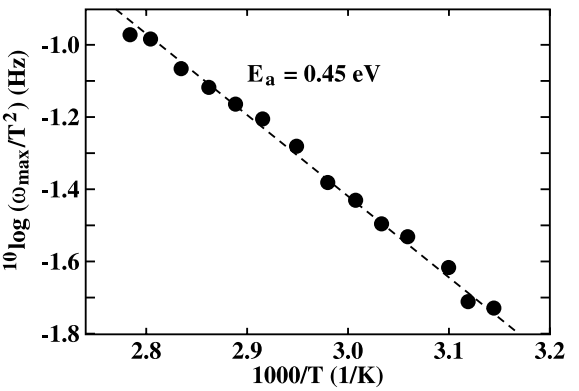

Fig. 13. Fit of the data of Fig. 12 gives an activation energy of 0.45 eV for these particular interface states seen at 1.5 V bias.

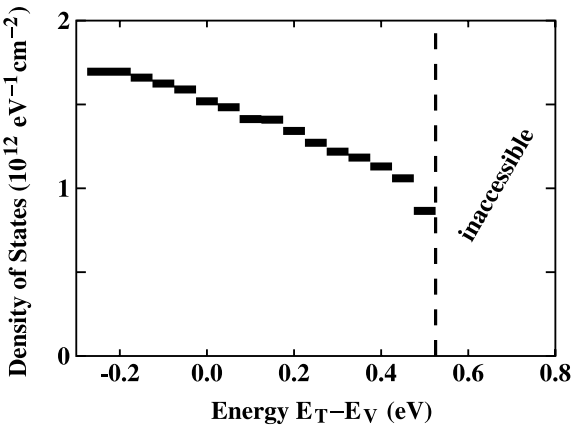

Fig. 14. Density of interface states in the forbidden gap as measured in the current work.

exactly 1 eV per V bias change and no voltage drop is absorbed by, for instance, the interface layer. Then the central position of the Fermi level can be calculated as $E_F = E_V + 0.45\ \text{eV} - q(V_b - 1.5\ \text{V})$. Also, we assume that the entire voltage modulation of 50 mV is translated into a Fermi level modulation of 50 meV. This assumption is used to be sure about the number of states contributing to the admittance. With this in mind we can map the interface state band. We are only limited by the fact that we do not observe a peak in loss or loss tangent below a forward bias of 1.5 V and hence states above $E_V + 0.45$ eV are not accessible. Using this method we arrive at the results shown in Fig. 14 and we find an increasing density of interface states closer to the band edge.

5. Discussion and conclusions

The accuracy of the measurements is limited at this moment. It is also hindered by the fact that wide bandgap materials such as most organic semiconductors are difficult to measure. At each series of measurements, the deep states reach a new occupancy and it takes a long time to reestablish equilibrium conditions. Ideally, before each scan, the sample has to be allowed to relax very long time, in the order of days. In reality, this is unpractical and the equilibrium conditions have to be sacrificed a little. This might be a cause for the error in the measurements. Note for example the two runs of Fig. 11. Each measurement gives slightly different results.

Also, the determination of the energetic position of the interface states in the forbidden gap is difficult, as demonstrated by Fig. 14 where some of the levels are predicted to lie below the valence band edge. A reason might be a relaxation of the lattice upon capture or emission of a carrier. This can make the thermal activation energy (the one that we measure) higher than the distance between the level and the valence band. However, a more likely explanation for the odd energy scale is the incorrectness of the assumption that the Fermi level moves exactly 1 eV/V with the bias. Very likely, part of the voltage drop is absorbed by the interface layer. The relation of activation energy with bias, as used in the text, is lost in that case. Ideally we should determine the activation energy via the temperature dependence at every bias. In practice this is unworkable due to the change of the device at every run. Finally, the method used for determining the activation energy of the states at 1.5 V forward bias (see Fig. 13) can be inaccurate. It is there assumed that the position of the Fermi level is independent of temperature and that we are therefore measuring the same states for all temperatures. In fact, free carriers are expected to freeze out and the Fermi level is expected to move with temperature. This makes that we are measuring (the relaxation time of) slightly different states at each temperature, even if the bias is the same, and Eq. (7) is not applicable. The activation energy is then different from the one measured.

We also want to mention that we have analyzed the device in a classical way, that is, as if the band edges are sharp and the value of E_V is well defined and homogeneous across the interface. In practice, the band edges might have a (Gaussian) distribution [20]. However, this would only cause a deterioration of the resolution of the energy scale, while the analysis remains the same. For this reason we have omitted such effects from our model.

In spite of this, the data show clear evidence for interface states. The fact that the states are distributed in space in a narrow region is shown by their peaked contribution to the conductance

when scanned over bias. Their rather homogeneous distribution in energy is shown by Fig. 14. The value of some 10^{12} $eV^{-1}\,cm^{-2}$ and the distribution in energy, higher density closer to the band edge, is very reasonable and comparable to other semiconductors such as silicon [1]. Less information exists about interface states in organic materials. Recently Berleb et al. use admittance spectroscopy to find evidence for trapped charge at an organic–organic interface, but no information is found as to the distribution of these charges in energy [21].

To summarize we have demonstrated how we can successfully show the presence of interface states in an organic semiconductor (in this case terrylene) using dc measurements and admittance spectroscopy techniques. The latter also gave an estimate for the density and energetical distribution of the interface states. To our knowledge, this is the first time that impedance spectroscopy was used to map interface state distributions in organic semiconductors.

Acknowledgements

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