Electronic transport in field-effect transistors of sexithiophene

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The electronic conduction of thin-film field-effect-transistors (FETs) of sexithiophene was studied. In most cases the transfer curves deviate from standard FET theory; they are not linear, but follow a power law instead. These results are compared to conduction models of "variable-range hopping" and "multi-trap-and-release". The accompanying *IV* curves follow a Poole-Frenkel (exponential) dependence on the drain voltage. The results are explained assuming a huge density of traps. Below 200 K, the activation energy for conduction was found to be ca. 0.17 eV. The activation energies of the mobility follow the Meyer-Neldel rule. A sharp transition is seen in the behavior of the devices at around 200 K. The difference in behavior of a micro-FET and a submicron FET is shown. © *2004 American Institute of Physics.* [DOI: 10.1063/1.1789279]

I. INTRODUCTION

Although electronics based on organic materials have many advantages, such as low cost of production, structural flexibility, and a wide range of materials with different properties, there are still many drawbacks that hinder a successful introduction to a larger share of the commercial market. Specifically, organic field-effect-transistors (FETs) differ in various ways from their inorganic counterparts.

(i) Currents depending supralinearly on the gate bias.

(ii) Nonlinear effects in the low-bias region of the *IV* curves.

(iii) Device metastability caused by the gate bias.

(iv) Reduced mobility.

The low mobility of the carriers limits the materials to low-frequency applications, while the device stability is a more serious problem and needs to be resolved before the next step in technology can be taken.

Nonstandard electrical characteristics are often explained in the literature with contact effects at the electrodes or barriers formed at grain boundaries. For the first we can imagine high-resistive regions at the contacts, causing voltage drops at the interface[1] and resulting in a saturation of the current upon increments in the gate bias,[2,3] or rectifying Schottky barriers formed by the electrode metal and the semiconductor, resulting in nonlinear currents in the low-drain-voltage regime. The grain boundaries can form barriers for current by trapping large densities of charge. These can also cause nonlinear effects in the currents.[4]

Another possibility is that traps are responsible for the nonstandard effects observed. Because of the wide band gap of most organic semiconductors, combined with their low purity and poor crystallinity, a huge number of deep, localized states are expected in these materials. These localized states — traps — can cause many reversible and irreversible effects on the behavior of the device. In this work we will show that traps can explain all our results of thin-film FETs based on vacuum-sublimed αT6. Although the alternative theories including grain boundaries or contact effects, can explain some of the results, they are not able to explain all of the results. Moreover, the ideas presented here are applicable to many semiconductor materials with low carrier mobility, in particular organic materials.

II. THEORY

In this section the various models to explain nonstandard *IV* curves and transfer curves are presented, including variable-range hopping (VRH), multi-trap-and-release (MTR), and Poole-Frenkel (PF). We start from standard FETs, in this case the currents follow:[5]

$$I_{ds} = \frac{W}{L} C_{ox}\mu(V_g - V_t)V_{ds} \tag{1}$$

in the linear region, with C_{ox} the insulator capacitance, L and W the device dimensions (distance between source and drain electrodes and length of electrodes, respectively), μ the mobility of the carriers, V_g and V_{ds} the voltage at the gate and drain, respectively, when the source is grounded, and V_t the voltage needed to open the channel. In other words, $C_{ox}(V_g - V_t)$ is the density of charge at the interface and μ the response (speed) of a carrier to the longitudinal field (V_{ds}/L).

Empirically, a deviation from standard theory can be described by

$$I_{ds} = \frac{W}{L} C_{ox}\mu(V_g - V_t)^{1+\gamma}V_{ds}, \tag{2}$$

with γ — normally positive — a parameter indicating the deviation from standard theory. Such behavior has been observed before[2] and explained by a MTR model or VRH theory.[6] In both models, currents are the result from a move-

ment of carriers from trapped state to trapped state. In VRH, the hop from one site to the next is limited by two factors: (i) wave function overlap and (ii) barrier height. The wave function overlap increases by the proximity of traps, but this is counteracted by the increased barrier height for closer sites. The result is a variable-range hopping of carriers. The MTR model is also based on a large number of traps, with the difference that the conduction is via delocalized band states. From the traps themselves no movement is possible. First a carrier has to be thermally activated into a delocalized-states band from where it can contribute to conduction. This theory is well described in the book of Shur in the section on amorphous silicon TFTs.[7]

In the model presented by Vissenberg and co-workers,[6] based on the VRH theory, an assumption is made of an exponentially decaying density of trap states, although the model predicts quantitatively similar results for other distributions. The outcome is that, when the *as-measured* mobility is defined as

$$\mu_{\text{FET}} \equiv \frac{L}{W C_{\text{ox}} V_{\text{ds}}} \frac{\partial I_{\text{ds}}}{\partial V_g}, \tag{3}$$

this mobility is

$$\mu_{\text{FET}} = \mu_0(T) V_g^{2(T_0/T-1)} \tag{4}$$

with T_0 a parameter describing the distribution of band-tail states. This model thus predicts an as-measured mobility, that is, depending on the temperature and the gate bias. Moreover, comparing Eq. (4) to Eq. (2) we can conclude that this model predicts a γ of the form

$$\gamma = 2(T_0/T - 1). \tag{5}$$

The MTR model similarly predicts a temperature-dependent mobility. To understand why it serves to analyze what happens when the gate bias is increased, free holes, initially induced by an increase of the gate voltage, are trapped onto the deep states. While still contributing to the capacitance charge $(Q = C_{\text{ox}} V_g)$, they no longer contribute to the channel current, $I_{\text{ds}} = \mu(V_g - V_t) V_{\text{ds}}$. If such trapping is (much) faster than the measurement scanning time, thermal equilibrium is reached during the measurement and a reduced effective mobility is measured. Since the steady-state ratio of trapped-to-free carriers depends on the temperature, the as-measured mobility becomes temperature dependent,[8]

$$\mu_{\text{FET}} = \mu_0 \alpha \exp(-E_T/kT), \tag{6}$$

with μ_0 the mobility of the carrier in the delocalized band, k the Boltzmann constant $(1.38 \times 10^{-23} \text{ J/K})$, α the ratio between the density of delocalized states to trap states, and E_T the distance between these two. Note that this mobility can still depend on the gate bias.[7] Another observation to be made is that, this temperature dependence is equal to the Poole-Frenkel model to be presented later.

On the other hand, if the trapping is slow, we can still observe effects of the traps in our measurements. A prolonged application of a gate voltage between scans will cause a threshold voltage shift ΔV_t that can be as large as the applied gate voltage — thereby completely quenching the channel current— if traps are abundant and deep, and man-

age to capture all induced free charges. Such so-called stressing has been observed before in T6[9,10] and amorphous silicon. Because the states responsible for trapping and quenching of the current do not have discrete levels or are abundant, a nonexponential decay of the current is observed in a transient (I_{ds} vs time). Such a decay can be expressed by a stretched-exponential[11,12] also known as glassy relaxation and already observed by Kohlrausch in the 19th century,[13]

$$I_{\text{ds}} = I_0 \exp[-(t/\tau)^\beta], \tag{7}$$

with $\beta \leq 1$ a parameter that approaches 1 for simple exponential decay, and τ the time constant of the relaxation. This behavior is common for materials with a large number of traps, such as amorphous silicon and organic materials, and even commercial GaAs FETs[14] can show nonexponential transients. With a large number of trap states the filling and emptying times of the traps are comparable resulting in transients as described above. When the trap levels are distributed in energy, a convolution of transients from the individual levels can also result in such nonexponential behavior.

An extended version of the MTR model is given by Poole and Frenkel.[5] This model includes the effect that the emission from the traps — and hence the effective mobility of the carriers — can be field dependent. In this case the field is the longitudinal field E_L caused by the drain-source voltage. (In the linear region the field is uniform in space and equal to $E_L = V_{\text{ds}}/L$.)

$$\mu = \mu_0 \exp\left[\frac{-q(\phi_B - \sqrt{qE_L/\pi\varepsilon})}{kT}\right]. \tag{8}$$

In this equation q is the elementary charge $(1.602 \times 10^{-19} \text{ C})$, ϕ_B is the trap depth, and ε the semiconductor permittivity. This causes a nonlinear dependence of the current on the drain-source voltage in the linear region of the IV curves; see, for example, the results presented by Waragai *et al.*[15] The ionization energy $q\phi_B$ of the trap can be found by studying the activation energy $E_A = q[\phi_B - (qE_L/\pi\varepsilon)^{1/2}]$ as a function of temperature and voltage. Comparing Eq. (8) to Eq. (6) we can see that the MTR model is a variant of the Poole-Frenkel model for low fields.

In the literature, sometimes nonlinear effects at low fields are attributed to Schottky barriers or high-resistive regions formed at the electrodes. Schottky barriers will show an exponential dependence of the current on the voltage, when the barrier is the limiting factor. Important to note is that when a Schottky barrier is formed at one electrode, an opposite barrier is formed at the counter electrode. Hence, one of them is always reverse biased and the maximum current of the device is a reverse-bias saturation current. Alternatively, a situation might exist where the Schottky barrier is the limiting factor and is controlled by the gate. The resulting device structure (junction FET) is significantly different from our metal-insulator-semiconductor field-effect-transistors (MISFET) structures, however.

Depending on the deposition methods, large contact resistance can be expected at the electrodes. Horowitz *et al.* pointed out that in these situations, saturation in the transfer curves can be expected, i.e., the current rises sublinearly with the gate bias.[3] They also describe a procedure for correcting
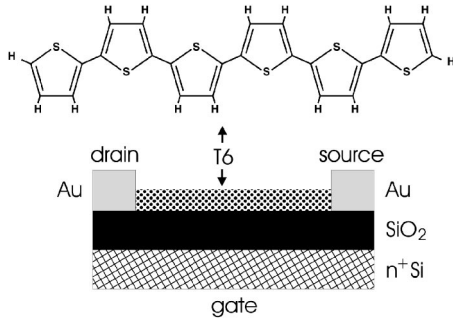
FIG. 1. Cross-section of the FET structure used in this work and a molecule of α-Sexithienyl, also known as α-Sexithiophene, or abbreviated as αT6.

this resistance. Recent studies describe a method for finding the contact resistance by studying the total device resistance as a function of channel length. The contact resistance can then be found by extrapolating to zero channel length.

In some cases, specifically in the case of granular materials, the currents in the *IV* plots and transfer curves, instead of being controlled by traps, can be governed by the grain boundaries either by the presence of wells[4] or barriers.[16] Moreover, it is often difficult to decide between a grain-boundary-barrier model and a trap model on the basis of experimental results. As discussed by Street *et al.*,[16] the evidence for the barrier model can be found in the linearity of the so-called Levinson plot, $\ln(I_{ds}/V_g)$ vs $1/V_g$ as well and the (positive) sign of the turn-on voltage.

Finally, for many organic materials the Meyer-Neldel rule holds. Without giving any physical explanation, this rule states that the as-measured mobility for any gate voltage, when presented in an Arrhenius plot, lies on a line going through the Meyer-Neldel point (T_{MN}, μ_{MN}). In an equation

$$\mu_{\text{FET}} = \mu_{MN}\exp[-E_A(1/kT - 1/kT_{MN})], \qquad (9)$$

with E_A the activation energy which can depend on the gate bias, and T_{MN} the isokinetic temperature. Chen and Huang[17] and Crandall[18] suggested a connection between the Meyer-Neldel rule and the stretched-exponential relaxation. Other authors suggested a link between the Meyer-Neldel rule and a field-dependent mobility.[19]

III. EXPERIMENTAL DETAILS

Thin films of α-sexithienyl (better known as α-sexithiophene, or αT6), see Fig. 1, were deposited onto preformed FET structures by vacuum sublimation. The FET structures consisted of gold electrodes on top of oxidized heavily-doped *n*-type silicon (oxide thickness 200 nm or 800 nm). Various channel widths and lengths were used. The smallest length was in a submicron FET, where the electrodes were fabricated by the stamping technique. All the measurements were done inside a cryostat at high vacuum, where the temperature could be stabilized down to ≈ 100 K.

IV. RESULTS AND DISCUSSION

Figure 2 shows typical *IV* curves of a long-channel device ($L=20$ μm) for various gate biases ranging form 0 to -50 V. Due to the low scanning speed of in this case
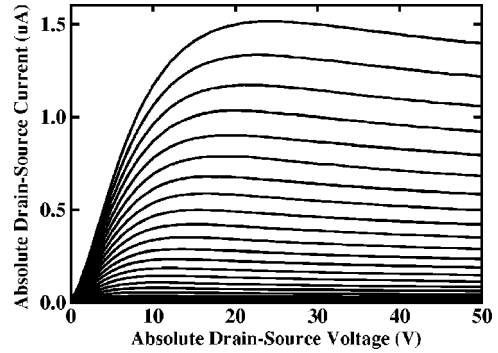

FIG. 2. Typical *IV* curves (I_{ds} vs V_{ds}) for various gate biases ranging from 0 to -50 V. The scanning was performed slowly ($dV_{ds}/dt=1$ V/s) resulting in a stressing during the measurements; a decay of the current after saturation. $W=20$ cm, $L=20$ μm, $d_{ox}=600$ nm. At the origin Poole-Frenkel conduction is responsible for the nonlinear current.

(1 V/s), trapping of free holes takes place during the measurements, thereby closing the channel. This is best seen in the saturation part of the curves, which show a decay of the current. Another detail is visible at the origin. Here a slight nonlinearity of the current can be discerned, indicating Poole-Frenkel conduction. The discussion of this will be postponed to later on the hand of devices that show this more clearly.

The same effect of trapping and stressing can be seen in the hysteresis measurements of a device in the linear region, see Fig. 3. The scan from 0 to -40 V lies above the subsequent scan from -40 to 0 V indicating trapping of charges or a similar process to be responsible for the decay effect. In the same figure it can be seen that the averaging of the up-scanning curve and the down-scanning curve does not result in a straight line. Apparently, the standard FET model of Eq. (1) does not apply. The MTR and VRH models predict such a nonlinear behavior, see Eq. (2). The VRH model predicts a current proportional to $V_g^{1+\gamma}$, with γ depending on the temperature as in Eq. (5). To test this model, the order of the root that linearizes each transfer curve was determined. To obtain this, first the threshold voltage was found through a fit to Eq.
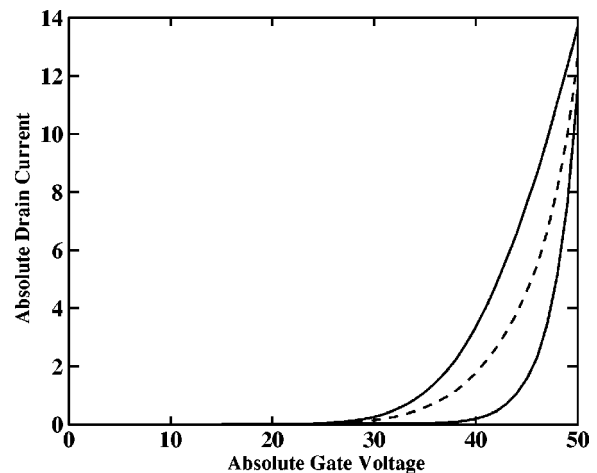

FIG. 3. Transfer hysteresis curve for $V_{ds}=-2$ V. The large hysteresis is caused by the stressing of the device. The dashed curve is the average of the two curves. Note that this is not linear and the standard FET model of Eq. (1) does not apply.
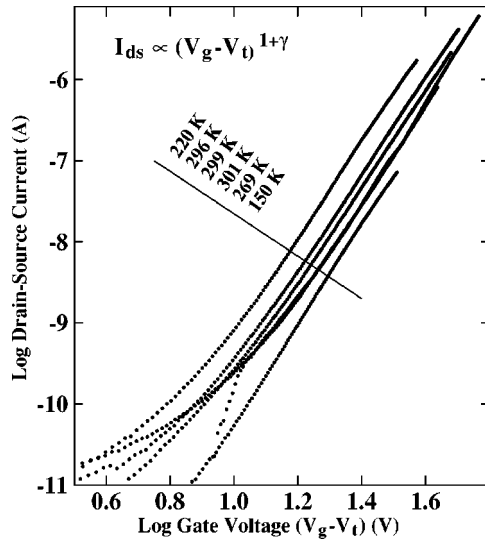
FIG. 4. Transfer curves at temperatures as indicated presented in a log-log plot. The gate voltage V_g was corrected for the threshold voltage V_t. To find V_t, a fit was made to Eq. (2). The slope of a curve is equal to $1 + \gamma$. For every temperature, γ is approximately equal to 5. This cannot be explained by the model of Vissenberg.

FIG. 5. Schematic representation of the idea that can explain a gate-dependent mobility. Density of free (p) and trapped (p_t) holes as a function of the position of the Fermi level (arbitrary scale). For $E_F > 0.6$ eV the ratio of free-to-trapped carriers depends on the Fermi level and this causes a gate-dependent mobility, as demonstrated in the text. Figure adapted for p-type FETs from Ref. 7. Note that the figure is not quantitatively applicable to the current work. The figure is merely used to explain the phenomenon of gate-bias-dependent mobility.

(2). This threshold voltage was then subtracted from the gate bias. The factor $1 + \gamma$ could then be found as the slope in a log-log plot. Figure 4 shows some examples of a particular device at several temperatures ranging from 150 K to 340 K. Clearly, γ is independent of temperature and remains fixed at ≈ 5 for this device. This directly contradicts the model of Vissenberg, which predicts a temperature dependence of γ as given in Eq. (5). However, the high value for γ can be explained with the MTR/PF model when the density of free carriers is insignificant compared to trapped carriers, but rises faster with the Fermi level at the interface and hence with the gate voltage, as demonstrated for amorphous silicon in the text book of Shur.[7] Following this reasoning, we can predict any value for γ: Imagine a situation where the density of trapped charges p_t depends on the position of the Fermi level in an exponential way [Eq. (10)], and the density of free holes p depends exponentially on the Fermi level in a different way [Eq. (11)], as shown in Fig. 5,

$$p_t = p_{t0} \exp(-aE_F), \tag{10}$$

$$p = p_0 \exp(-bE_F). \tag{11}$$

Here a and b are parameters that describe the dependence (b is nominally $1/kT$ as for simple conduction and valence bands). The induced total charge density at the interface depends on the gate bias, $Q_{tot} = C_{ox} V_g = p_t + p$. The conduction, however, is only caused by free holes $I_{ds} \sim p$. Now if the density of trapped charge is much higher than the density of free charge, $p_t \gg p$, then a combination of Eqs. (10) and (11) will result in a gate-dependent mobility μ_{FET}.

$$I_{ds} \propto C_{ox} V_g^{b/a} V_{ds}. \tag{12}$$

Hence, $\gamma = b/a - 1$. The factors a and b (can) depend on the position of the Fermi level. As an example, in Fig. 5, when the Fermi level is below 0.5 eV, both slopes are parallel and $\gamma = 0$, whereas when E_F is above 0.6 eV, γ is much larger
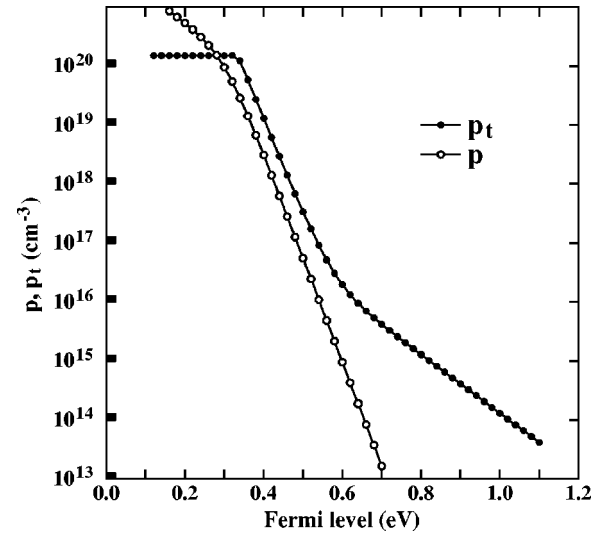
than 0. Once the channel is formed, the gate bias will move the Fermi level relatively little at the interface, and we can expect the currents to follow the above equation for a wide range of gate biases. The temperature, however, can move E_F significantly, resulting in a temperature-dependent γ. (The density of trap states is not expected to depend on temperature, otherwise it would also be a source for a temperature-dependent γ.) This can encompass the behavior as described by Vissenberg and co-workers[6] or Shur[7] and Eq. (5) when the density of deep states grows exponentially over a wider energy range.[7] Moreover, the density and energetic distribution of the traps and thus the parameters a and p_{t0} can strongly depend on the device fabrication and handling conditions and even on the history of the device, making γ vary from sample to sample and in the extreme cases even from measurement to measurement. It still remains to be explained how the value of γ can be totally independent of temperature *and* deviating from zero as demonstrated in Fig. 4. Possibly, a huge density of traps pins the Fermi level at a certain point.

The as-measured mobility as a function of temperature is presented in Arrhenius plots in Fig. 6 for various gate biases. The procedure here was to fit the transfer curve with a model of Eq. (2) at each temperature. From this, the as-measured mobility was calculated with the definition of Eq. (3). As can be seen, the device follows the Meyer-Neldel rule for temperatures below 200 K with a T_{MN} of Eq. (9) of 750 K and a prefactor $\mu_{MN} = 0.37$ cm^2/Vs. Above 200 K the device switches abruptly. While the Meyer-Neldel temperature remains at 750 K, the prefactor drops to 2.6×10^{-2} cm^2/Vs. The temperature of 200 K coincides with the onset of stressing as previously described by us.[9] While both effects — stressing and a nonzero γ — are caused by traps, the direct link between the two is not clear at this moment. In the literature for amorphous silicon stressing is explained by as-
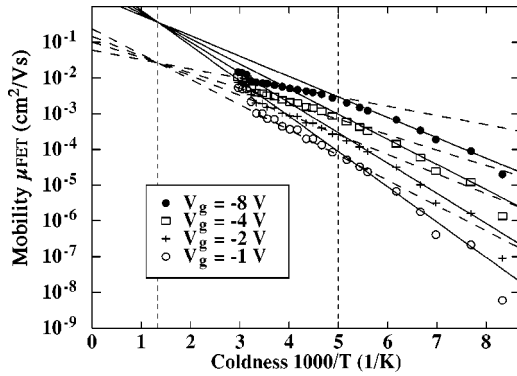
FIG. 6. Arrhenius plots of the as-measured mobility μ_{FET} for various gate voltages $V_g - V_t$. The Meyer-Neldel rule holds with a transition at around 200 K. The median activation energy for the lines shown above is 0.16 eV, close to the activation energy found in the temperature-scanned-current measurements.

FIG. 8. Arrhenius plot of the as-measured mobility of a submicron-FET for various gate biases.

suming a *creation* of new defects, while, as shown above, for a gate-dependent mobility only the *existence* of trap states is needed.

Other devices measured showed similar behavior. In some devices γ nearly follows the theory of Vissenberg, with a T_0 of Eq. (5) of ≈ 400 K, whereas other devices deviate more from this theory, with the extreme case the one presented above. One of the devices measured in this study had a short (submicron) channel length and therefore deserves a little more attention in this report. Figure 7 shows γ as a function of temperature. In this case, a sharp transition of γ is seen at 200 K. This transition is even more pronounced in the Arrhenius plots of the mobility, see Fig. 8. Such sharp behavior is typical for a phase transition; however, more information is needed to draw such a conclusion.

In some cases the current might be limited by the barriers formed at the grain boundaries. According to the potential barrier model, the currents follow the equation[16]

$$I_{ds} = \frac{W}{L} C_{ox} \mu_0 V_g' \exp(-s/V_g') V_{ds}, \tag{13}$$

with V_g' the gate voltage corrected for the threshold voltage. Here s is a parameter that depends on the temperature but not on V_g. Thus, a Levinson plot of $\ln(I_{ds}/V_g')$ vs $1/V_g'$ will result
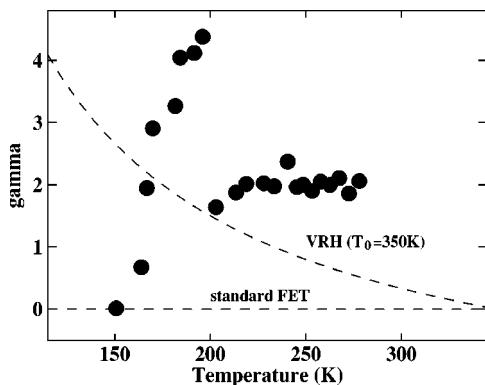
in a straight line if the model is applicable to our devices. Figure 9 shows such a Levinson plot for a long-channel FET where a lot of barriers might be expected. On the basis of this figure the potential-barrier model seems unsustainable. Moreover, the same reasoning about the (negative) sign of the turn-on voltage of the devices can be employed as used by Street *et al.*[16] to reject the barrier model.

For low conductivity materials, Poole and Frenkel suggested a field-assisted hopping via traps as the conduction model in 1938. In this case, the conduction is via a delocalized band, but most of the time the charge spends at localized states. Equation (8) describes the field dependence of the mobility and Eq. (6) describes the temperature dependence. Note that these models assume that only the mobility depends on temperature while other parameters (such as the threshold voltage or trap density) do not. The activation energy E_T of Eq. (6) for a device at a certain bias can be found by plotting the thermally activated current in an Arrhenius plot. Figure 10 gives an example. In this case, the current grows exponentially with an activation energy of 170 meV below 200 K. Above 200 K the stressing starts, as described elsewhere.[9] The creation of new trap states causing the threshold voltage shift is now faster than the exponential ionization from the traps and, therefore, the current drops.

Clearer evidence for Poole-Frenkel conduction can be

FIG. 7. Dependence of γ in $I_{ds} \sim (V_g - V_t)^{1+y}$ on the temperature of a submicron-FET. A sharp transition is seen at 200 K. The dashed curves show simulations of the behavior as predicted by Vissenberg with $T_0 = 350$ K and standard FET theory.
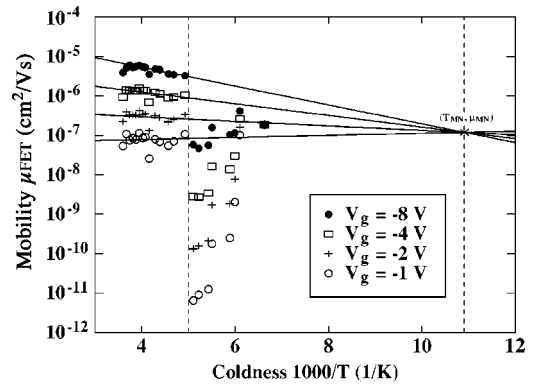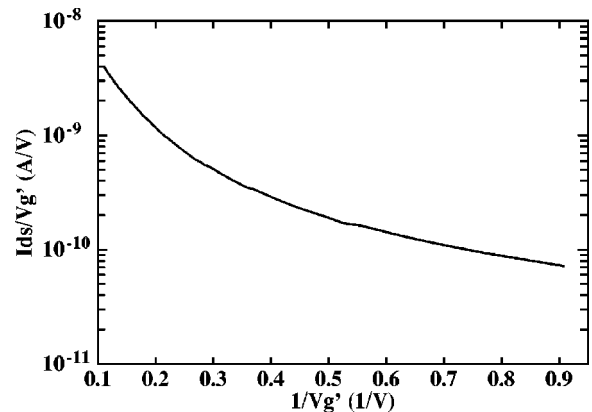
FIG. 9. Levinson plot of a device at a temperature of 150 K. The curve has been corrected for the threshold voltage $V_g' = V_g - V_t$ with $V_t = -1.0$ V, as found by Eq. (2). The nonlinearity of the curves hints at a failure of the barrier model. Absolute values of currents and voltages used.
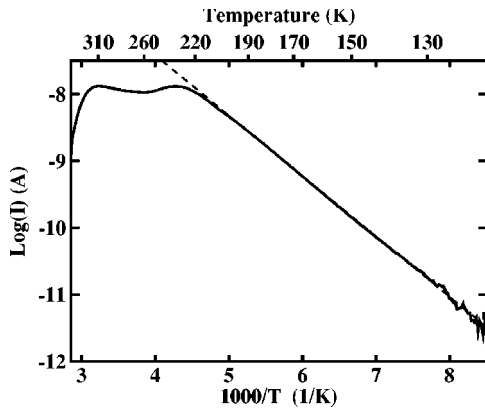
FIG. 10. Arrhenius plot of the current. The current below 200 K can be perfectly fit with activation energy of 170 meV. Since the mobility is only weakly longitudinal and transverse field activated (see, for example, Figs. 10 and 5, respectively), this energy is close to the trap depth, E_T. At 200 K the stressing starts creating a large threshold voltage, as described elsewhere (Ref. 9). Scanning parameters: $V_{ds}=-0.5$ V, $V_g=-9$ V, $dT/dt=45$ mK/s.

found in the low-voltage regions of the *IV* curves. Equation (8) predicts a current that depends supra-linearly on the drain-source voltage in the low-field region. Moreover, these effects are expected to be most pronounced at low temperatures. Figure 11 shows some *IV* curves similar to the ones in Fig. 2, but of another device at 140 K. The curves are shown in a form $\ln(I_{ds}/V_{ds})$ vs $V_{ds}^{0.5}$, which should be linear according to Eq. (8) (Note: $I_{ds} \propto \mu V_{ds}$). As can be seen, the Poole-Frenkel model describes the current very well. Theoretically, substituting the mobility of Eq. (8) in Eq. (1), the slope of this curve should be equal to (units SI)

$$\frac{\partial \ln(I_{ds}/V_{ds})}{\partial \sqrt{V_{ds}}} = \frac{q}{kT}\sqrt{\frac{q}{\pi\varepsilon L}} = 0.89 \text{ V}^{-1/2}, \tag{14}$$

(based on $L=10$ μm, $T=140$ K, and $\varepsilon=5\varepsilon_0$). The experimental slope obtained from Fig. 11 is 0.29 V$^{-1/2}$, reasonably close to the theoretical value. The difference might be due to an underestimation of the value of ε of T6 in the thin-film structures. Another idea that might occur is that the Poole-Frenkel type conduction applies to only a small part of the device (interface regions), with, therefore, a much shorter L. In that case, however, the value of the slope should increase beyond the theoretical value of 0.89. Therefore, we see no
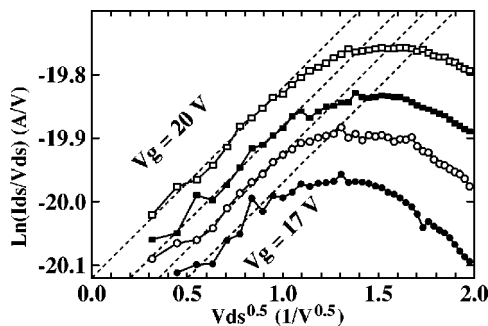

FIG. 11. *IV* curves at 140 K for different gate biases ranging from -17 V to -20 V. This shows that the Poole-Frenkel model applies. Note: the curves have been shifted vertically in order to be closer to the $V_g=-20$ V curve. Device dimensions: $L=10$ μm, $W=10$ mm.
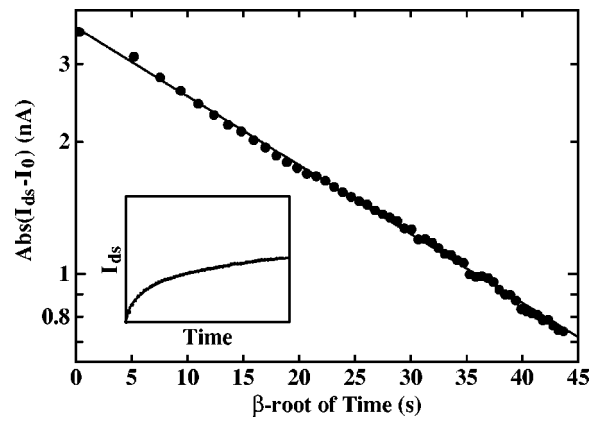

FIG. 12. Current transient for $V_g=-10$ V and $V_{ds}=-5$ V. The straight line is a fit with near square-root behavior, $\beta=0.5391$. The inset shows the same data and fit in linear format.

proof of a PF conduction limited to only certain regions of the device.

Traps are also efficiently studied in current transients. For a discreet, low-density trap level the free charge is expected to decay exponentially. Moreover, a low density of traps or a shallow trap is not able to remove all the gate-induced free carriers from the delocalized band, and the current saturates at a nonzero value

$$I_{ds} = \Delta I \exp(-t/\tau) + I_0 \tag{15}$$

with $\tau=\tau_0\exp(-E_T/kT)$. The trap level can then be found by determining τ as a function of temperature. However, in this case of a low density of deep traps, capacitance methods, such as DLTS, are more adequate.[20,21]

It is interesting to note that to measure the intrinsic mobility μ_0 of the material the measurement should be done faster than the trapping time to ensure measuring the initial current. This, however, requires ultra-fast-pulsing techniques. In slow scanned dc operation, the steady state I_0 current is measured and a reduced effective mobility μ_{FET} is found, which is a weighed average of mobility of carriers in the delocalized band and the trap states. Using intermediate speeds can result in any value of the mobility measured ranging from μ_0 to μ_{FET} of Eq. (6).

When the density of traps is large, the decay is no longer simple exponential. The same can happen when the states responsible for the trapping are distributed in energy or the density of traps is changing over time. In that case, the relaxation becomes a convolution of relaxations to each trap state. The result of this is the so-called stretched-exponential transient of Eq. (7).[11,13]

Figure 12 shows a transient for a gate voltage of -10 V and a drain-source voltage of -5 V. The current follows a perfect stretched-exponential decay with a β of 0.54 when an offset current is subtracted. For other devices, the value of β normally falls in the range 0.25–0.5, but in most cases β is close to 0.5 and the offset is negligible, i.e. the channel closes, indicating a huge number of traps.

Research is currently underway in our group to determine the nature of the traps. First results hint at an energetic distribution of traps causing the nonexponential transients.

V. CONCLUSIONS

The results presented in this work can be explained when a huge density of trapped charge compared to the density of free holes is assumed. From this follows a gate-dependent mobility $\mu = \mu_0 V_g^\gamma$, a stressing of the device (a shift of V_t over time making it approach the gate bias) and a stretched-exponential behavior of the transients. Because of the abundance of trap states, whenever there are free charges, eventually they will all be trapped (marginally closing the channel, $V_t = V_g$). Moreover, a model incorporating a large density of traps also adequately describes the longitudinal-field-dependent mobility according to the Poole-Frenkel model $\mu = \mu_0 \exp(a V_{ds}^{1/2})$. As an example of the activation energy of the current we found a value of 0.17 eV. It is not directly clear if this value relates to the trap depth. It is also important to note that this energy is not necessarily equal to the energy of defect creation found in the stressing experiments.[9]

The model of Shur, via Eq. (12) predicts a mobility that depends on the gate of the form $\mu \propto V_g^{b/a-1}$. In this way, the explanation of the gate-dependent mobility has been postponed to explaining the factors a and b. As said before, b is normally $1/kT$, as for normal band conduction. For the factor a we expect the same value, independent of the distribution of the trap states, when the Fermi level is far above the trap level. Only in the case of a Fermi level resonant with the trap level can we expect a factor a smaller than this (and hence a supralinear growth of the current in a transfer curve).

On the other hand, the model of Vissenberg and co-workers based on the VRH theory — without the inclusion of delocalized bands, but only an exponentially decaying tail of trap states — does not adequately describe all of the devices.

The Meyer-Neldel rule that states that the mobilities as plotted in an Arrhenius plot for any gate bias lie on a line going through a single point holds for all samples, with a transition at 200 K. In the nano-FET this transition is most abrupt and dramatic. This transition is also visible in the temperature-scanned currents; at 200 K the creation of new defect states eclipses the effect of ionization of charges from the already existing traps. Hence the current drops rapidly.

A Levinson plot of the transfer curves revealed that barriers at grain boundaries are not needed to explain the behavior of the devices. Also, in no case was contact resistance needed to describe the data.

It has to be pointed out that, although the results presented here were obtained for αT6 FETs, similar results can be expected for other materials. As long as the trap density is huge compared to the density of free states, similar behavior is expected; gate-bias-dependent mobility, stressing, and Poole-Frenkel conduction. In a forthcoming publication, we demonstrate that a large density of trap states also causes the observation of the Meyer-Neldel rule.[22]

As to the origin of the traps, nothing can be decided on the basis of the results presented here. However, since a truly abundant trap is needed, an intrinsic defect is expected rather than an impurity. As to the location of the traps also not much can be said, but these traps should be in the vicinity of the channel accommodating the current. The most likely place is in the organic layer, at the interface.

One final thing to remark is that when we talk about the behavior of the mobility, such as activation energy etc., we are in fact talking about the behavior of the density of mobile charges. The real mobility of the free charges is constant and much higher.

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