ADVANCED MATERIALS

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Metal–Insulator–Metal Transistors**

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Electronic devices, especially non-linear ones, are normally fabricated from semiconductor materials, prominently silicon. Moreover, the transistor, an essential element in both analog and digital electronics, has had a tremendous impact on our society. One can say that it has revolutionized the world in just a couple of decades. This was all made possible by the unique and necessary properties of semiconductors. Or so it seems. Here it is shown that, in the so-called thin-film transistor architecture, any material can be used to fabricate a switching device. As an extreme case, a transistor is presented in which the active layer is made of a metal, to result in a metal–insulator–metal transistor. The devices have normal field-effect transistor characteristics and have some interesting advantages over their semiconductor counterparts, for example, an infinite on–off ratio and no lower limit to the dimensions of the devices, apart from a general enhanced flexibility in design.

One class of transistors is the so-called field-effect transistor (FET). They consist of a metal (the 'gate') and a semiconductor (the 'active layer') to which the drain and source electrodes are connected laterally to inject and collect carriers. Separating these two layers is an insulator. One of the most famous is the MOS-FET,[1] so named after the materials used for the three layers: metal, oxide, and semiconductor. Any bias applied to the gate causes charge in the semiconductor, to form a so-called 'channel'. This charge increases the conductance of the semiconductor layer and the current from source to drain. It can thus be said that the gate is programming the resistance of the channel in the semiconductor, hence trans-resistor, or 'transistor' for short. As a result of technological advantages, modern devices are often thin-film transistors (TFTs), the majority of which are made of silicon.[2] They differ from the MOS-FETs in that the active layer, though still made of a semiconductor, is thin. It has been shown experimentally that a single monolayer of material suffices.[3] Figure 1 shows a schematic picture of a TFT.

The TFT has some advantages such as flexibility of production. As an example, in contrast to a three-dimensional MOS-FET, TFTs can be produced by printing, either ink-jet printing or stamping. While this is especially true for organic materials,[4,5] inorganic materials can also be produced in such a way.[6]

On the other hand, TFTs have a major disadvantage, namely lower speeds caused by the reduced charge carrier mobility, which finds it's origin in the huge density of traps (localized electronic states) inherent to amorphous materials, which in turn is caused by the lattice mismatch between the materials used for the insulator and active layer. However, this disadvantage is rapidly disappearing as technology is improved; field-effect mobilities show a sharp upward trend over the last decades[7] and now reach the 1 $cm^2 V^{-1} s^{-1}$ range, which is sufficient for low-frequency applications. These same traps also cause a large threshold (switch-on) voltage in TFTs that makes them incompatible with real applications. Thus, as a side effect of the increased mobility, the threshold voltage is also reduced and TFTs become ever more commercially viable. This reasoning applies equally to organic and inorganic materials and even mixtures of the two have been suggested for the active channel,[8] which makes the number of possible devices virtually unlimited.

The operating voltage is further decreased by using alternative dielectrics for the insulating layer;[9] where TFTs have more flexibility in choosing the material, a high dielectric constant (k value) can be used. For comparison, the silicon oxide relative permittivity $\varepsilon_r = 3.9$ and alternative dielectrics can have k values up to 100.[10] The operating voltages inversely scale with the k value and this gives organic materials the edge.[11] A suitable choice for the insulator also allows for the reduction of leakage current to the gate. Other technological barriers, such as the need for ambipolar transistors for logic elements also seem to have been tackled.[12,13] There seems to be nothing preventing (organic) thin-film transistors to have a bright future,[14,15] where 'bright' can even be taken literally, as in light-emitting field-effect transistors.[16]

In spite of the increasing popularity of the TFT, the same MOS-FET model has been used to describe them, since, empirically, this seems to do quite well. It has been shown, though, that this is less adequate for two simple reasons: 1) A MOS-FET needs band bendings (curvatures of the energetic diagram in space) caused by ionized acceptors or donors, yet, in practice, acceptors and donors are not needed to make a TFT

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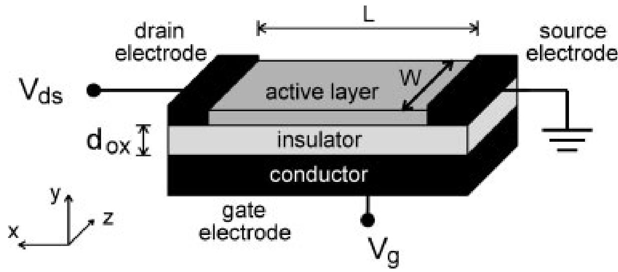

Figure 1. Cross section of a thin-film FET showing the nomenclature used in the current work.

work. Moreover, such band bendings, for any reasonable dopant concentration, take several hundreds of nanometers of space, which is orders of magnitude more than the thickness of the device. 2) MOS-FETs work in inversion, meaning that the charge responsible for electronic transport in the channel is of opposite sign compared to the charge in the bulk, whereas TFTs conventionally work in accumulation (same-sign charge in bulk and channel). Thus TFTs merit their own modeling.[17] The single postulate needed is effectively treating the device as a parallel-plate capacitor in which the charge density, $\rho(x)$, at any place x along the channel, is given by the local potential drop across the insulator (here called oxide for historical reasons) multiplied by it's capacitance density ($C_{ox} = \varepsilon_{ox}/d_{ox}$, with ε_{ox} the permittivity and d_{ox} the thickness of the oxide layer), namely

$$\rho(x) = C_{ox}[V(x) - V_g] \tag{1}$$

where $V(x)$ is the local potential in the channel at position x, and V_g is the potential at the gate. (See Figure 1 for a schematic TFT device and the nomenclature used in this work.) When substituting this in a differential equation in which the local current (I_x) is equal to the free charge density (considering that all charge is free charge), the charge carrier mobility (μ), the device width (W), and the local field ($-\mathrm{d}V(x)/\mathrm{d}x$),

$$I_x(x) = -\rho(x) W \mu(x) \frac{\mathrm{d}V(x)}{\mathrm{d}x} \tag{2}$$

and solving it with boundary conditions ($V(0) = 0$, $V(L) = V_{ds}$, and $I_x(x) = I_{ds}$, where I_{ds} is the external observable current), the result is behavior very similar to MOS-FET devices, yet with a more adequate starting point, since no band bendings or dopants are needed. The fact that these are not needed and, as a result, that devices can be as thin as one monolayer, opens the way for some peculiar devices, since, as a direct result from our model, it is foreseen that there are nearly no limitations to the material that can be used for the active layer. Any material can be used that has a non-zero charge-carrier mobility and a band structure such that a barrier exists at the interface to prevent the relevant charge from leaking back to the gate.

In fact, a bandgap is not even needed and it was thus predicted, by taking the model to the extreme, that a metal can be used for the active layer. For metals, however, a term, $-qn_0$, has to be added to the right hand side of Equation (1), which represents the zero-bias free-electron density multiplied by elementary charge (charge neutrality at zero bias is maintained by the compensating positively charged host matrix). To guarantee a good relative modulation effect of the gate bias, this term has to be kept as low as possible; for instance any additional layer(s) beyond the first cannot be affected by the gate field and thus reduce the effectiveness of the TFT by supplying a parallel conductance path. In other words, for metals, it is essential to have the active layer as thin as possible.

A device was thus fabricated with such a metal active layer (see experimental). Ultra-thin gold layers could be made with, for the thinnest films, a varying coverage of the substrate. Figures 2 and 3 show examples of output curves (I_{ds}–V_{ds}) for several key thicknesses of the gold film. For devices without a gold film, currents are below the noise limit (Fig. 2). For a device with ~30% of the insulator in the channel covered by gold, the gate effect is pronounced and the currents can be completely switched off for moderate biases (see Figs. 3a and 3b). A (sub)mono-layer device (~50% coverage of the insulator by gold, see Fig. 3d) shows a lower (relative) gate

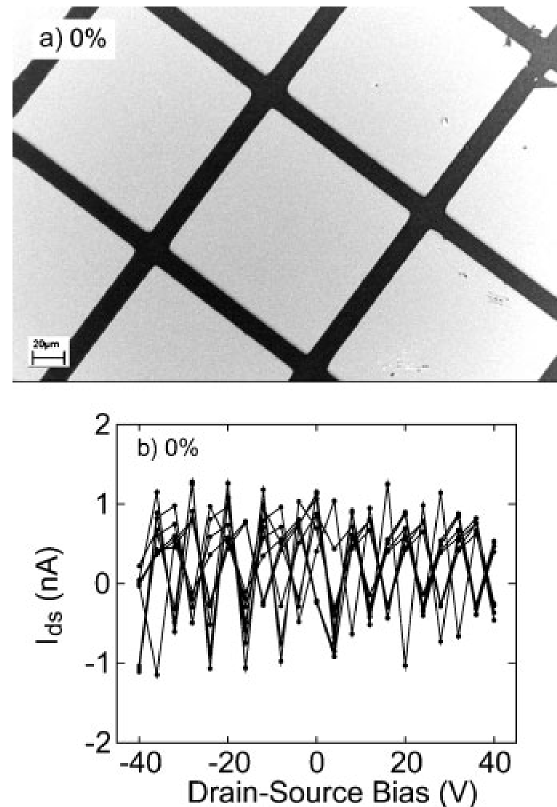

Figure 2. a) SEM image of a pristine device with the gold electrodes only (without gold film). The light square areas are the gold contacts/electrodes and the dark lines are the channels. b) The corresponding I–V output curves for gate biases from −40 to 40 V showing that leakage currents are below the noise level.

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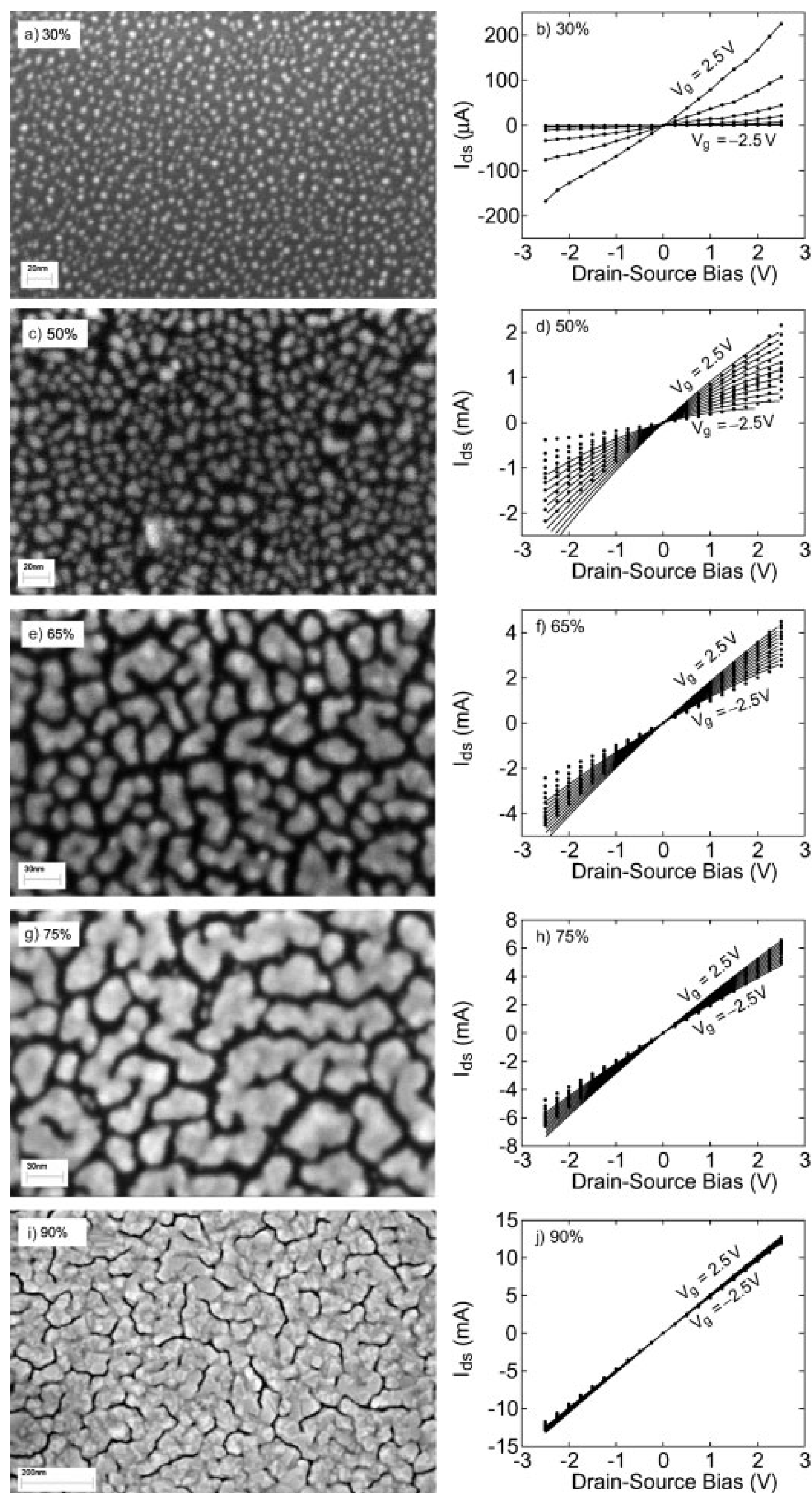

Figure 3. Typical SEM images (a, c, e, g, i) and corresponding *I*–*V* curves (b, d, f, h, j) for indicative stages of gold-film coverage. a,b) (Sub)mono-layer device, 30% coverage (the lines are to guide the eye). c,d) 50% coverage showing a good gate effect (the lines are simulations with $n_0 = 1 \times 10^{16}$ m^{-2} and $\mu = 600$ cm^2 V^{-1} s^{-1}). e,f) Increased coverage (65%) (solid lines: simulations with $n_0 = 2.45 \times 10^{16}$ m^{-2} and $\mu = 600$ cm^2 V^{-1} s^{-1}). g,h) Increased coverage (75%) with a reduced gate effect owing to the large presence of free carriers in the metal (solid lines: simulations with $n_0 = 3.8 \times 10^{16}$ m^{-2} and $\mu = 600$ cm^2 V^{-1} s^{-1}). i,j) 90% coverage where the gate effect and the switching behavior of the resistor is nearly absent and the device works more like a thin-film resistor (solid lines: simulations with $n_0 = 16 \times 10^{16}$ m^{-2} and $\mu = 295$ cm^2 V^{-1} s^{-1}).

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effect and the channel is no longer closed for reverse bias. Simulations of the currents for this device are shown in the figure with parameters of $n_0 = 1 \times 10^{16}\ \mathrm{m}^{-2}$ and $\mu = 600\ \mathrm{cm}^2\ \mathrm{V}^{-1}\ \mathrm{s}^{-1}$, the latter being a reasonable value for the mobility of bulk gold. Increasing the coverage to approximately 65 and 75% decreases the relative gate effect further because of the increased value of n_0 to 2.45×10^{16} and $3.8 \times 10^{16}\ \mathrm{m}^{-2}$, respectively, while maintaining the same mobility value. (Note the larger absolute value of the current, thus drowning the gate effect, see Figs 3e to 3h). In all cases, positive gate biases open the channel and this confirms the fact that the carriers responsible for conduction are electrons (the only mobile charges available in metals). Finally, for a 90% covered device the relative gate effect is nearly absent (see Figs. 3i and 3j) because of the large 'background' density of electrons. The device starts behaving like a thin-film resistor.

By analysing the data, it can be seen that the effect of better coverage of the substrate by the gold film is mainly an increase in density of electronic states, n_0, which increased by a factor of 16 from 30 to 90% coverage. The simulations have been optimized for the positive side of the bias. For the negative side the fitting is of lower quality. Note also that, apparently, the density of states n_0 does not scale linearly with the coverage of the substrate (from 50 to 90% coverage it increases a factor 16 instead of 1.8).

Even more remarkable is the fact that while the channel can be closed completely by a strong enough gate bias, as evidenced by Fig. 3b for the thinnest coverage (30%), there is no sign of saturation in the *I–V* curves. For semiconductor TFTs these two effects — channel closing and saturation in *I–V* curves — go hand in hand since they are two manifestations of the same thing. In this simple model, diffusion of carriers is ignored and this might explain some discrepancies between the model and experimental results.

Finally, the value of n_0 is very low. Extrapolating from the bulk density-of-states (DOS), a monolayer of gold should have a DOS of approximately $1.2 \times 10^{19}\ \mathrm{m}^{-2}$. These issues are currently not well understood and need to be studied further. Yet, there is no doubt as to the field effect of the device and that it depends on the film coverage.

The transfer curves of the devices with 30 and 50% coverage are shown in Figure 4. For the 30% covered device, the transfer curves are highly non-linear ($\propto V_g^{7.6}$), which indicates that traps play a dominant role[17,18] (traps are not included here in the simplified model). On the other hand, the transfer curve of the 50% covered device is linear, which shows that this device behaves more like an ideal transistor. The threshold voltage is not an adjustable parameter in this model (only n_0 and μ are), but instead follows from the other parameters, $V_T = -qn_0/C_{ox}$; it is the voltage needed to drive out all the free charge. Using the value of $n_0 = 10^{16}\ \mathrm{m}^{-2}$ found before in the output curves (for the 50% device) yields $V_T = -4.6\ \mathrm{V}$; a fit to the transfer curve gives a close value, $V_T = -4.3\ \mathrm{V}$. The on–off ratio is theoretically infinite. In practice the determination of this value is difficult because of the large experimental noise and

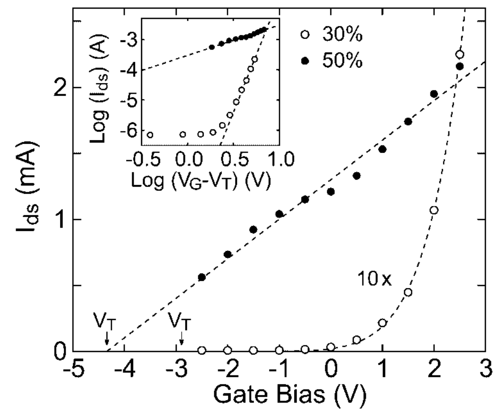

Figure 4. Transfer curves at $V_{ds} = 2.5$ V for the device with 30% coverage (o, multiplied by 10) and 50% coverage (•). The dashed lines are linear ($I_{ds} \propto (V_g - V_T)$) and power-law ($I_{ds} \propto (V_g - V_T)^\alpha$) fits to the transfer data. The indicated threshold voltages V_T are derived from the fit. The highly non-linear transfer curve for the 30% covered device ($\alpha = 7.6$) demonstrates the prominent role of traps. [17, 18] The inset shows the same data in a log–log scale adequate for power-law functions. An on–off ratio of about 400 can be seen here for $V_g = \pm 2.5$ V, limited by a leakage or instrumental current in the sub-microamp range.

leakage. For the 30% covered device it lies around 400 for $V_{ds} = 2.5\ \mathrm{V}$ and $V_g = \pm 2.5\ \mathrm{V}$.

One thought that might occur is that the operation of the metal–insulator–metal transistor is based on the presence of barriers at the source and drain electrodes that can somehow be programmed by the gate. Note, however, that in our devices the electrodes and the active layer are made of the same metal and thus no barriers can exist. The functionality is purely attained by charge-modulation effects of the gate bias; the field at the gate attracts or repels charges in the channel.

In summary, the idea originating from the TFT model that a transistor can be made out of any material has been taken here to the extreme and it has been demonstrated experimentally that a thin-film transistor can be made with a metal for the active channel. Other materials can also be used, with some minor limitations: i) The energetic bandgap of the material of the active layer cannot be wider than that of the insulator, but can be zero, as in metals. ii) For conductive materials, the active layer has to be as thin as possible, preferably one monolayer in order to prevent parallel conductance. For materials without free carriers, no such limitations exist and they can be as thick as desired. iii) The charge carriers should have reasonable mobilities to make sure that charge induced in the channel actually can contribute to current.

While the TFT was used here as a proof-of-concept device to demonstrate the validity of the two-dimensional model and its preference over the more widely used MOS-FET model, the metal TFT has some unexpected advantages which are listed below together with the advantages of TFTs in general as emerging naturally when bearing the model in mind:

- The metal TFT theoretically has an infinite on–off ratio because the gate field can completely drive out the electrons

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from the active layer. This occurs at a threshold voltage of $V_T = -qn_0/C_{ox}$, below which the current is zero. (Experimentally a value of 400 is observed, Figure 4, probably because of leakage currents and a high noise level). This is a clear advantage over it's semiconductor counterpart in MOS-FETs where the subthreshold current is exponentially dependent on the bias[1] and can thus never be switched off completely. For commercial devices, the on–off ratio is an important figure-of-merit.

- The experimental metal TFT shows no non-linearities such as saturation, even if this is not theoretically well understood.
- For a metal TFT, the channel can be made of the same material (metal) as the source and drain contacts and this further increases device simplicity and reduces the cost of production.
- A TFT, as envisioned here, has no contact effects,[19] which increases the number of possible materials for use for the connections. For classical transistors, the choice of materials for the contacts is limited to avoid unwanted rectifying properties of the interfaces.
- Because there are nearly no limitations as to the choice of material for the active layer, including, as has been shown, metals, the active layer can be more easily optimized for price, non-toxicity, speed of production, structural flexibility, bio-compatibility, etc.
- For the same reason, sensors are envisaged in which the active layer is optimized more easily for sensing.
- In contrast to the MOS-FET, there are no limitations as to the size of the device. For a MOS-FET, band bendings (perpendicular to the surface and at the contacts) are essential, and the minimum size is in the order of 100 nm. In TFTs, as has been argued, there are no band bendings or depletion zones (for the metal TFT this is obvious, but this also can be shown for other TFTs[17]) and there is no lower limit to the device dimensions. True molecular TFTs are within the realm of possibility,[20] whereas they are impossible in the framework of MOS-FETs.[21]

In conclusion, it has been shown here how to fabricate a metal–insulator–metal field-effect transistor, something that has been expected for some time but until now has not been achieved. The trick lies in the reduction of the density of states by not fully covering the substrate. This increases the relative field effect. Moreover, the advantages of this metal TFT and the expected results of TFTs in general when they are (treated as) true two-dimensional devices have been argued. This is an important finding for enabling progress in both organic and inorganic TFTs. It is obvious that a lot of work still has to be done in both experimental and theoretical aspects. Take, for example, the less-than-perfect rudimentary simulations with only two parameters that can only explain some features of the electrical behavior.

Experimental

Devices with a metal active layer and dimensions $W = 100\,\mu m$ and $L = 15\,\mu m$ were fabricated. A common substrate–gate structure thin-film transistor was made in the following way. An oxide SiO_2 layer (100 nm, relative permittivity = 3.9) was thermally grown on heavily doped n-type Si substrates (the gate electrode). Subsequently, source and drain electrodes (50 nm thick) and monolayer and multilayer films were thermally evaporated by using a grid shadow mask. Scanning electron microscopy (SEM) images of Au-electrode-only structures are shown in Figure 2. Electrical measurements were performed with a Keithley Model 4200-SCS Semiconductor Characterization System. The pristine devices as shown in Figure 2 had negligible current. The values for percentage coverage of the device, as mentioned in the text, were found by optical estimation. In all, more than 40 devices with different thickness, as mentioned in the text, have been fabricated to check the reproducibility of the device performance, which systematically resulted in the behavior described here.

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