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Electrical characterization of CVD diamond–n^+ silicon junctions

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Abstract

The electrical characteristics of CVD-diamond/n^+-Si heterojunction devices are reported. Below 250 K the diodes show an unusual inversion of their rectification properties. This behavior is attributed to an enhanced tunneling component due to interface states, which change their occupation with the applied bias. The temperature dependence of the loss tangent shows two relaxation processes with different activation energies. These processes are likely related with two parallel charge transport mechanisms, one through the diamond grain, and the other through the grain boundary. © 2001 Elsevier Science B.V. All rights reserved.

Keywords: CVD diamond; Electrical properties; Heterojunction

1. Introduction

The large-scale development of diamond-based electronic devices relies on the use of polycrystalline films, which can be deposited in a reproducible way, on large surface and on the conventional substrates used in silicon based microelectronics. Silicon substrates are therefore often used, and a number of devices have been reported [1–6].

An interesting structure is a cold cathode field emission device, which uses highly doped n-type silicon as one of the electrodes. These silicon/CVD diamond heterojunctions, have an energy barrier at the interface. Because the silicon is highly doped, most of the depletion region occurs in the diamond side. Therefore, these abrupt asymmetric junctions resemble Schottky barrier devices, and should play a role in the supply of electrons to the diamond. However, most of the field emission studies using silicon substrates [3–6] focus their attention on the effects of diamond composition, structure, and morphology, on the turn-on voltage for field emission. The electrical properties of the silicon/diamond interface are usually neglected, and some reported results in DLC materials show that the back contact has little effect on the emission threshold field [7].

Field emission involves not only the process of emission at the diamond surface, but also the supply of electrons to the material, and the transport through the bulk. Therefore, it is also necessary to have a good understanding of the mechanisms of electrical injection of carriers and transport through the silicon/diamond interface.

In this paper we report on a investigation of the electrical characteristics of diamond/n^+-Si heterojunction devices. The results of these experiments reveal

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that, interface states play a dominant role in determining the electrical characteristics of the devices in agreement with a previous work by Wang et al. [2].

2. Experimental procedures

The diamond films were grown, on n-type silicon wafers with a bulk resistively of 0.1 Ωcm, in an RFA microwave-plasma-assisted chemical vapor deposition (MPCVD) system. The gas composition was 1% methane (CH_4) and 99% hydrogen (H_2), at a pressure of 40 torr, and a temperature of 800°C. The total time of deposition was 14 h. The silicon substrate had been pre-treated by polishing with diamond powder of 0.25-μm grain size and cleaned in a ultrasonic cleaner before deposition. The resulting film has a thickness of approximately 5 μm, as shown by an infrared interference measurement. Gold was evaporated on top of the diamond through a mask to form an array of circular electrodes (2 mm in diameter). For the electrical measurements the devices were mounted in a temperature-controlled sample holder located inside a steel chamber evacuated to less than 10^{-5} mbar. Small-signal admittance measurements over the range 50 Hz–1 MHz were carried out with a Fluke PM 6306 RCL meter. The DC I–V curves were recorded with a Keithley 487 Picoammeter/voltage source. The sample temperature was varied in the range 100–400 K and measured with a platinum resistor.

3. Results and discussion

3.1. Diode characteristics

Experimental evidence for the existence of a thin depletion layer on the diamond side is provided by the capacitance–voltage (C–V) measurements. As a typical result, the $1/C^2 - V$ characteristics measured at 200 Hz are shown in Fig. 1. The voltage dependence of the junction capacitance is due to changes in the size of the depletion region. The effective acceptor concentration, N_A can be graphically obtained from the slope of the figure, resulting in 2×10^{17} cm^{-3}. In order to shed light on the conduction mechanisms in our diodes, the current-voltage characteristics were measured in the temperature range 119–400 K. Typical results are shown in Fig. 2. The forward-bias characteristics are roughly exponential up to 1 V above which they start to be limited by the diamond bulk series resistance. The poor rectification ratio is due to the non-saturating of the reverse bias current.

A particularly interesting feature of these diamond devices is their behavior at low temperatures. Looking again at Fig. 2, it can be seen that the I–V plots have inverted rectification at low temperatures. Below 250 K, the reverse bias current is higher that the forward

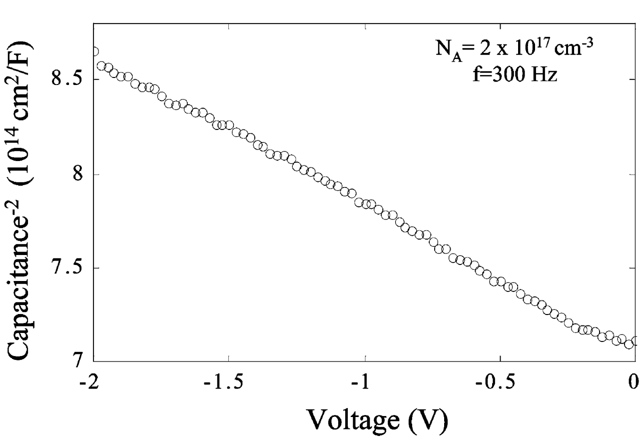

Fig. 1. Reciprocal capacitance squared vs. bias, recorded at a frequency of 300 Hz.

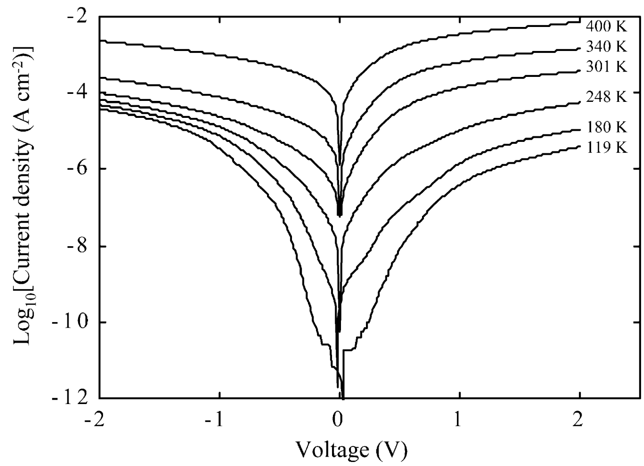

Fig. 2. Temperature dependence of the current-voltage characteristics.

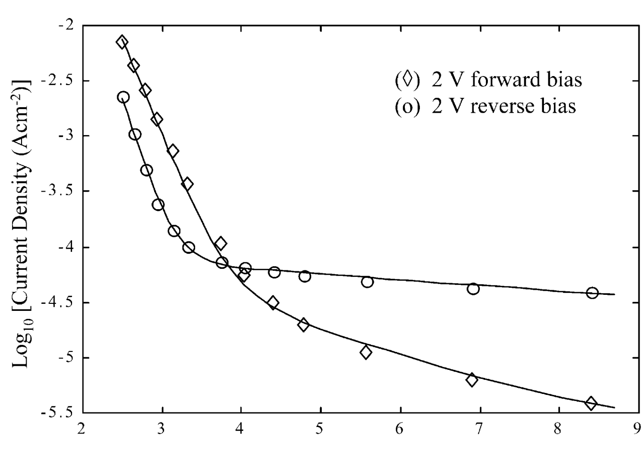

Fig. 3. Arrhenius plot of the current recorded under an applied bias of (◇) 2 V forward bias, and (○) 2 V reverse bias.

Table 1
Fitting parameters for both curves in Fig. 3 using the equation in the text

Applied voltage (v)	J_1 (Acm^{-2})	J_{01} (Acm^{-2})	J_{02} (Acm^{-2})	$E_{a1}(J)$ (eV)	$E_{a2}(J)$ (eV)
−2	7.0×10^{-6}	970	1.0×10^{-4}	0.45	0.012
+2	1.8×10^{-6}	190	33×10^{-5}	0.35	0.052

bias current. This unusual effect is clearly visible in the Arrhenius plots of the current, for both forward and reverse voltage of |2V|, given in Fig. 3. The two curves cross each other at the transition temperature of 250 K.

This transition temperature also marks a change in the charge transport mechanism. As already noted at the temperature dependence of the I–V curves, below 250 K the diode current is only slightly activated while about it is strongly activated. A reasonable fit was obtained using:

$$J = J_t + J_{01}\exp\left\{\frac{E_{a1}}{kT}\right\} + J_{02}\exp\left\{\frac{E_{a2}}{kT}\right\}$$

Where E_{a1} and E_{a2} are the activation energies, J_{01} and J_{02} are constants; k is Boltzmann's constant, and T is the absolute temperature. The fitting parameters for both curves are given in Table 1.

From a fit we obtain 12 meV for the activation energy at low temperatures and under a reverse bias of 2 V. Such small temperature dependence indicates a form of tunneling. We believe that the responsible mechanism is via states-assisted tunneling. The origin appears to lie in the presence of surface and near surface states or in the grain boundaries. The J–V characteristics for various temperatures were measured and the activation energies of the current were obtained for several voltages. For low applied bias, the activation energy is 0.55 eV. This is equal to the barrier height at zero bias. With increasing reverse bias the activation energy decreases, following a $V^{1/2}$ dependence, as can be seen in Fig. 4 where the activation energy is plotted vs. $V^{1/2}$. This kind of behavior has been found by Maeda et al. [9,10] in a-Si:H Schottky diodes. These authors have developed a model where non-ideal J–V characteristics of Schottky barriers are due to changes in population of the interface states under applied bias and accompanying changes of the barrier height.

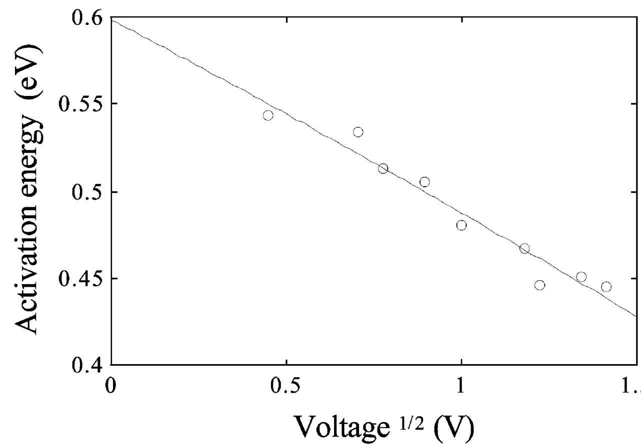

Fig. 4. Decrease of the activation energy, E_A for the reverse current vs. $V^{1/2}$.

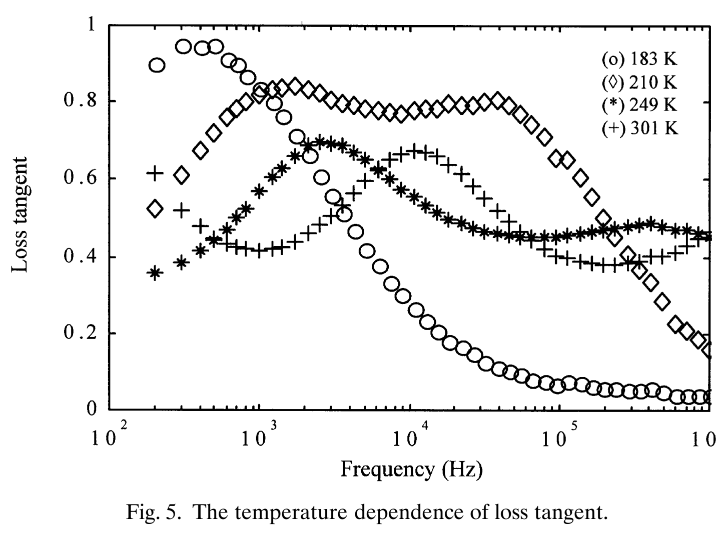

Fig. 5. The temperature dependence of loss tangent.

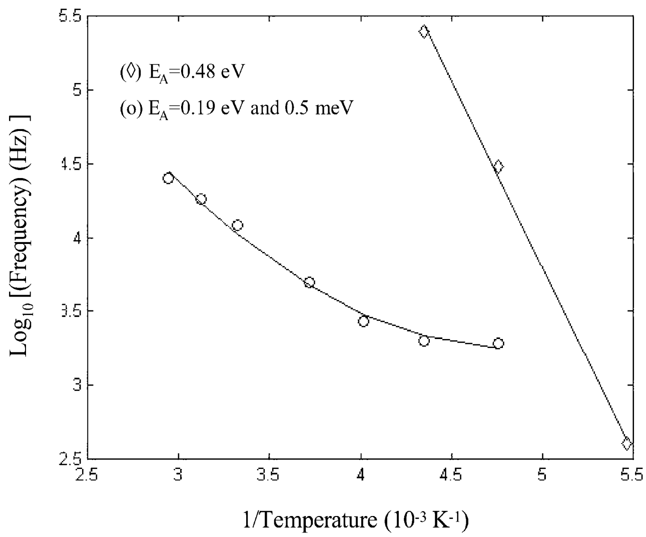

Fig. 6. Arrhenius plot of the frequency position of the peaks in the loss tangent of Fig. 5. The plot reveals an activation energy of 0.48 eV for the high frequency peak and of 0.19 eV for the low frequency peak.

3.2. ac properties

When measuring the ac impedance it must be remembered that a diode comprises a high resistivity layer (the depletion layer) in series with a low resistivity layer (bulk diamond) which has its own capacitance C_b and resistance R_b. Therefore, the measured capacitance cannot simply be assumed to arise solely from the depletion region. In general the results are interpreted in terms of an equivalent circuit taking both regions into account [8]. In Fig. 5, Tan $\delta = 1/(\omega RC)$, is plotted as a function of frequency and temperature. Tan δ shows two peaks. These maximums move to lower frequencies with decreasing temperature, and at low temperatures they cannot be completely observed in the measured frequency window. We believe the two peaks are associated with two different relaxation processes because they have distinct temperature dependence (see Fig. 6). The temperature dependence of the low-frequency peak has a behavior similar to the one displayed by the I–V curves, that is, it is weakly temperature-dependent below approximately 250 K but it is thermally activated (0.2 eV) at room temperature. In contrast, the high frequency peak seems to have a single activation energy with a higher value (0.48 eV), in the temperature range studied.

4. Discussion

The I–V characteristics of CVD diamond/n^+Si heterojunction show that tunneling is a predominant current transport mechanism below 250 K. This mechanism is enhanced under reverse bias, and this causes the existence of excess current and an unusual inversion of the diode rectification properties. We believe that the underlying mechanism is via states-assisted tunneling. The origin appears to lie in the presence of surface and near surface states, or in a highly defective region of the semiconductor near the interface. This process effectively bypasses the Schottky barrier and may be viewed as being in parallel with the barrier transport mechanisms.

The existence of interface or near surface states that change their occupation with applied bias seems to be supported by the observation that the barrier height decreases with the applied reverse voltage according to $V^{1/2}$ and in agreement with a model proposed by Maeda et al. [9,10].

It is well known that polycrystalline diamond is a non-homogeneous material with a current flow predominantly via the grain boundaries. Therefore polycrystalline diamond diodes are well described as a micro-cluster of paralleled junctions with different barrier heights. A natural approach is to assume the presence of two barrier heights, one associated with crystalline grains, and the other associated with the highly defective grain boundaries. The existence of two diodes in parallel explains the two different relaxation frequencies in the admittance spectra. The low frequency peak is likely to be due to the diode established with the diamond grain and the high frequency peak is related to the interface of the diamond material in the grain boundaries.

5. Conclusions

Heterojunctions resulting from an intimate contact of n^+ silicon and diamond deposited by MPCVD, have been studied by admittance spectroscopy and current-voltage measurements. The loss tangent show two relaxation processes, related with the non-homogeneous nature of the polycrystalline diamond films. It is assumed that the diamond diodes are well described by a micro-cluster of two parallel diodes, one associated with crystalline grains, and the other associated with grain boundaries. The I–V curves show that below 250 K there is weak temperature dependence, indicating a form of tunnelling transport. This mechanism is enhanced when a reverse bias is applied to the device, and causes an inversion of the diode rectification properties. It is proposed that the underlying mechanism is a tunnelling assisted via states near the silicon/diamond interface.

Acknowledgements

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References

[1] X. Jiang, M. Paul, C.P. Klages, Diam. Relat. Mater. 5 (1996) 251.
[2] W.N. Wang, N.A. Fox, T.J. Davis, J.W. Steeds, Recent Prog. Diam. Electron. (1998) 189.
[3] W.N. Wang, Proceedings of the 4th NIRIM International Symposium on Advanced Materials, (1997) 53.
[4] Y.T. Jan, H.C. Hsieh, C.F. Chen, Diam. Relat. Mater. 8 (1999) 772.
[5] S.S. Profffit, S.J. Probert, M.D. Whittfield, J.S. Foord, R. Jackman, Diam. Relat. Mater. 8 (1999) 768.
[6] A.V. Karabutov, V.D. Frolov, S.M. Pimenov, C.I. Konov, Diam. Relat. Mater. 8 (1999) 763.
[7] A. Hart, B.S. Satyanarayana, E.I. Milne, J. Robertson, Diam. Relat. Mater. 8 (1999) 809.
[8] L. Pereira, H.L. Gomes, A.M. Rodrigues, E. Pereira, Recent Prog. Diam. Electron. (1998) 243.
[9] K. Maeda, I. Umezu, H. Ikoma, T. Yoshimura, J. Appl. Phys. 68 (1990) 2858.
[10] H. Ikoma, K. Maeda, Jpn. J. Appl. Phys. 30 (1991) 19.