META-STABILITY EFFECTS IN ORGANIC BASED TRANSISTORS

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Abstract

Gate bias-induced stress has been investigated on sexithiophene-based ransistors. It was found that both a negative and a positive threshold voltage shift can be induced. Temperature-dependent measurements show that there are two processes involved in the negative threshold voltage shift, one occurring at T 220 K and the other at T 300 K. These two transition temperatures were interpreted in terms of a polaron mechanism associated with defects. The time and the electric field dependence of the threshold voltage were also studied.

INTRODUCTION

One of the most important stability issues in organic transistors is the shift in the threshold voltage upon applying a prolonged bias to the gate electrode, so-called stressing. Devices suffering from gate-bias stress effects exhibit threshold voltage shifts .V_{th}, currentvoltage characteristics with hystheresis and a slow and continuous decrease in the device current. Bias stress effects have been reported for a variety of organic based thin-film transistors (TFTs) [1-6]. In an attempt to understand the physical origin of this instability, several authors studied the effect using different dielectric materials [1,3], different types of silicon oxide as well as different surface treatments [6]. Some authors have reported that the time dependence of .V_{th} upon stress, follows a logarithmic law, and used this as evidence for traps located in the dielectric material [4,5]. We have shown that the logarithmic law is only obeyed for relatively short times. For stressing times upon 10^4 s the time dependence of .V_{th} follows a stretched–exponential behaviour

[8]. The data available in the literature suggest that stress in organic based devices is related to the properties of the organic semiconductor itself.

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Supporting this view is the observation that stress can be relaxed when the device is illuminated with band-gap light [6,7]. Street *et al.* [7] suggest that the effect arises from the formation of trapped bound hole pairs (bipolarons). The formation of these bipolaron states depletes the accumulation channel of mobile holes causing an increase in the threshold voltage. Since the polaron binding energy can be dependent on the structural disorder and impurities such as oxygen, this model explains readily how the device stability can be dependent on the sample preparation and handling.

In this article we studied the temperature and gate field dependence of the stress mechanism and discuss that in the light of polaronic species trapped by defects at the polymer/dielectric interface.

RESULTS AND DISCUSSION

The α-sexithiophene (α-T6) thin films were deposited by thermal sublimation in a ultra-high vacuum organic molecular beam deposition apparatus (base pressure (10^{-9} mBar) onto pre-formed TFT test substrates, consisting of a heavily n-doped silicon gate electrode, a 200 nm thick (thermally grown) SiO_2 insulating layer (C_{ox} = 19 nFcm^{-2}) and a patterned gold layer as the source and drain electrodes. The channel dimensions were *W/L* = 20,000 µm/10 µm. During the deposition, the sample substrate was held at 150ºC. All the electrical measurements were carried out in vacuum (10^{-6} mBar)

The transistors used in this study exhibit good characteristics with field effect mobility in the order of 10^{-2}cm^2/Vs. The output characteristics (I_{DS}-V_{DS}) show current saturation as well as negligible contact resistance (see Fig. 1.)

Figure 2 shows three transfer characteristics of a typical device measured in the linear region (V_{DS}= –0.5 V). Theses curves correspond to three states, designated here as (a) biasannealed, (b) equilibrium, and (c) stressed state. When devices are left resting for long periods of time (longer than one day), they exhibit a transfer characteristic designated here as the

equilibrium or relaxed state. This curve will suffer a parallel shift to higher threshold voltages without any variation of the subthreshold slope or the transconductance, if a negative gate bias is applied; we say the device becomes stressed. Gently heating the device to 340 K with a positive gate bias applied will bring the threshold voltage to a positive value (bias-annealed state). The transfer curve will correspond to a device, which has a channel open for $V_g = 0$ V, and it is usually know as a "normally on" FET. Furthermore, there is a residual off-state leakage current of about 0.1 nA, which decays with time following a stretched-exponential type behaviour. The ΔV_{th} shift is large for negative biasing and slight for bias-annealing.

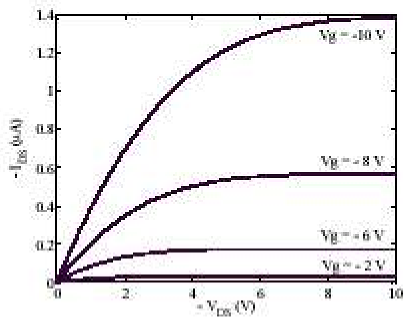

Fig. 1. *Drain current against drain voltage characteristics measured for a range of gate voltages applied to a sexithiophene transistor.*

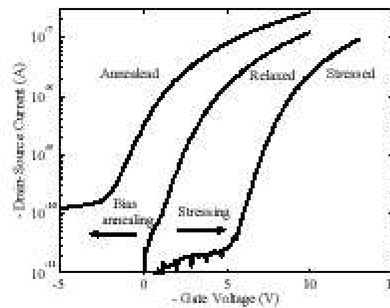

Fig. 2. *Transfer curves obtained for* $V_{DS} = -0.5$ V.

The changes between the three states are entirely reversible. The bias-anneal state will relax to the equilibrium state in a time scale of a few minutes (2-3 minutes). The kinetics of the stressed state has been previously reported by us to follow a stretched exponential behaviour [8], in agreement with a phenomenological description used in studies of stability in a-Si TFTs [9-11]. Using this formalism, a defect creation energy of $E_A \approx 0.52$ eV was obtained for sexithiophene based devices. This result agrees well with the estimated bipolaron biding energy as reported by Street *et al*. [7].

In order to shed some light onto the possible mechanism causing stress, the

temperature dependence of the drain current was measured for different gate voltages. The results are shown in Figure 3. In these experiments the relaxed devices are first cooled down to 100 K without bias and then, while the drain current is being measured in the linear region ($V_{DS} = -0.5$ V), they are heated to 340 K with a heating rate of 2.4 K/min with various gate biases.

For all gate voltages the drain current initially increases with the temperature, as

expected. However, at approximately 220 K the current passes through a maximum before decreasing with further rise in temperature. This decrease in current is caused by a continuous increase in the device threshold voltage. Therefore, we conclude that the stress-induced threshold voltage shift occurs only above 220 K. Below this temperature we observe that the threshold voltage is stable. Above 280 K the device current increases again before a second maximum sets in at around 300 K. In the temperature range [280–300 K] the current tends to recover. Above 300 K the current sharply decreases and stress effects dominate again. These results suggest there are two mechanisms involved. A low temperature process, which sets in at 220 K and room temperature a process occurring approximately at 300 K.

Fig. 3 also shows that in the temperature range [220–280 K] the higher the applied gate field, the less pronounced is the decrease in current caused by stress. To study this behaviour in detail the device was stressed at a fixed temperature for different gate voltages. The results are shown in Fig. 4. The current decrease induced by the threshold shift becomes slower for high gate fields. This interesting result may shed some light into the nature of the stress mechanism. While in the bipolaron model stress is proportional to the induced carrier density and therefore to the applied gate voltage, it is also true that under high electric fields, the charges are separated and it will be more difficult to form immobile bipolarons.

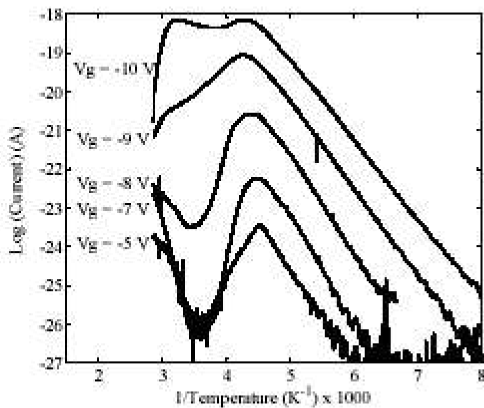

Fig. 3. Temperature dependence of the drain current, when the device is subjected to different gate voltages.

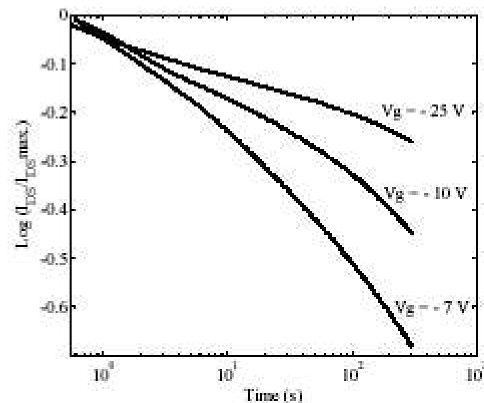

Fig. 4. Time dependence of normalized drain-source, for different gate voltages applied. Measurements done for V_{DS} = -0.5 V at the temperature of 260 K.

Subsidiary experiments have shown that the low temperature stress process correlates well with a thermal detrapping current which can be recorded by freezing a stressed device to 100 K and then warming-up it to room temperature with a defined heating ramp, while the short-circuit drain-source current is recorded. The polarity of this detrapping current can be reversed by applying a positive gate bias at 340 K (bias anneal procedure) prior to cooling down.

We suggest that the first stressing process is due to a defect which, when the device is operated in accumulation, can trap negatively charged carriers (polarons). This state can apparently also trap positive charge carriers when the temperature is high enough (340 K) and when a positive gate bias is applied (bias-annealing procedure). When positively charged this defect is responsible for the bias-annealed state.

The sharp threshold voltage shift observed above room temperature is likely to be due to the contribution of a deeper state, which probably traps double negatively charged polarons. One possibly origin for this defect state is a material phase transition.

In conclusion, a polaron mechanism associated with two types of defects is proposed to explain the temperature and gate field dependence of the threshold voltages shifts in sexithiophene-based transistors. However, further studies are needed to elucidate the nature and the location of these defects.

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