Meta-stability effects in organic based transistors

H. L. Gomes [*a], P. Stallinga [a], M. Murgia [b], F. Biscarini [b] T. Muck [c], V. Wagner [c]
E. Smits [d] and D. M. de Leeuw [d]

[a] University of Algarve, Faculty of Sciences and Technology
Campus de Gambelas, 8000 Faro, Portugal
[b] CNR- Istituto per lo Studio dei Materiali Nanostrutturati
Via P. Gobetti 101, I-40129 Bologna, Italy
[c] School of Engineering and Science, International University Bremen, campus ring 8, 28759 Bremen, Germany
[d] Philips Research, Prof. Holstlaan 4, 5656 AA Eindhoven, Netherlands

ABSTRACT

The electrical stability of metal insulator semiconductor (MIS) capacitors and field effect transistor structures based in organic semiconductors were investigated. The device characteristics were studied using steady state measurements AC admittance measurements as well as techniques for addressing trap states. Temperature-dependent measurements show clear evidence that an electrical instability occurs above 200 K and is caused by an electronic trapping process. It is suggested that the trapping sites are created by a change in the organic conjugated chain, a process similar to a phase transition.

Keywords: Organic transistor, gate-bias stress, traps, impedance spectroscopy.

1. INTRODUCTION

The technological applications of organic thin film transistors (OTFTs) are limited by the low mobility and by stability problems. Whereas the low mobility is not a severe limitation for low frequency applications, the electrical stability reduces the lifetime of the circuits. The most important stability issue in organic transistors is the shift in the threshold voltage upon applying a prolonged dc bias to the gate electrode, so-called gate-bias stress. Devices suffering from stress exhibit threshold voltage shifts ΔV_{th} and a slow and continuous decrease in the device current.
Bias stress effects have been reported for a large variety of materials [1-6]. In an attempt to understand the physical origin of this instability, several authors studied the effect using different dielectric materials [1-3], different types of silicon oxide as well as different surface treatments [6]. The data available in the literature suggest that stress in organic based devices is related to the properties of the organic semiconductor itself and is independent of the choice of gate dielectric, but no definitive evidence has been provided that charge trapping occurs in the organic or in the insulator or whether both mechanisms have contributed. Such a lack of distinction between the possible sources of the threshold voltage shift leaves room for conjectures about the quality of the active layer in the transistor, as opposed to the insulator layer. To solve this ambiguity, we have used simultaneously a metal-insulator-semiconductor (MIS) capacitor and an MISFET transistor structure fabricated in the same substrate to investigate the threshold voltage instability. Impedance techniques in MIS capacitors can provide information about the trap location in the device geometry and about trap properties by measuring changes in the diode impedance associated with carrier capture and emission processes at the trap state.

This article is also focused on the anomalous temperature dependence of the stress mechanism. Recently we showed [7, 8] that gate-bias-stress effects have complex temperature dependence, dominated by two processes, one occurring near 220

* hgomes@ualg.pt; phone: +315 289 800 900; fax: +315 289 819 403.

K and the other close to room temperature. A detailed study of this temperature-dependence is presented. Furthermore, different conjugated materials and polymer blends were compared with respect to their electrical stability. It is argued that the abrupt transition occurring near 200 K can be caused by a structural change in the molecule, such as a ring twist. Since some materials can be more prone to this changes than others, this can put new constrains in selecting conjugated materials for transistor applications.

2. EXPERIMENTAL

Several conjugated organic semiconductors were used in this study. The α-sexithiophene (α-T6) and dihexylquaterthiophene (DH4T) thin films were deposited by thermal sublimation in an ultra-high vacuum organic molecular beam deposition apparatus. Poly(3-hexythiophene) (P3HT) and [6,6]-phenly-C61-Butyric acid methyl ester (PCBM), were deposited by spin coating. Transistor test substrates were fabricated from a heavily n-doped silicon wafer with a thermally grown SiO_2 insulating layer and a patterned gold layer as the source and drain electrodes. The substrates were also treated with hexamethyldisilazane (HMDS), a surface treatment known to passivate the SiO_2 surface. Typical channel dimensions were W/L = 20,000 μm/10 μm. All the electrical measurements were carried out in vacuum (10^{-6} mBar).
AC admittance measurements were made using a Fluke PM 6306 LCR meter over the frequency range 50 Hz to 1 MHz. The signal amplitude was 400 mV.

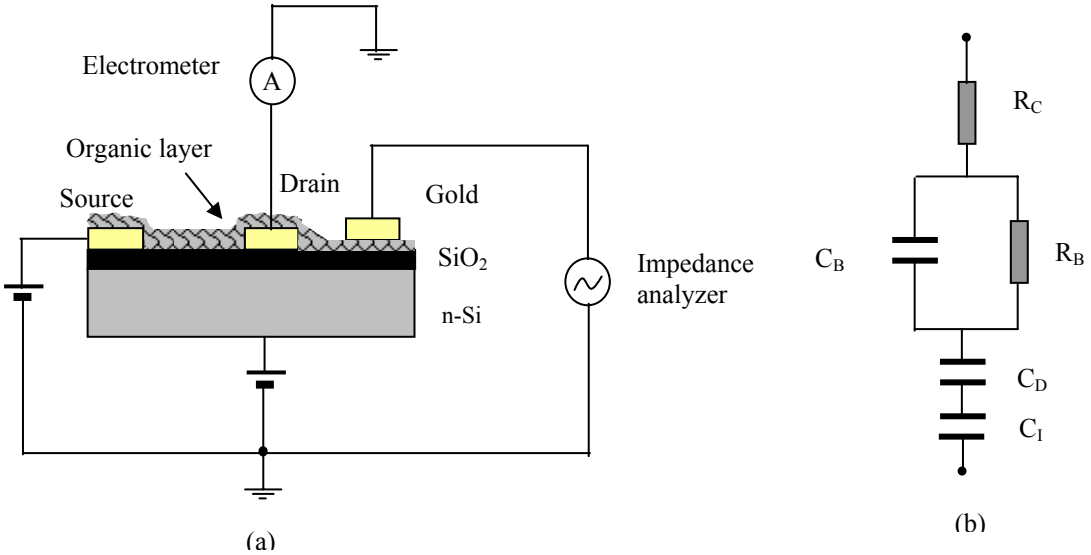

Fig.1. (a) Schematic diagram of the device structure used and (b) equivalent circuit representing an ideal polymer MIS capacitor.

3. RESULTS

3.1 Steady-state characteristics and the temperature dependence.

The transistors used exhibit good characteristics with field effect mobility in the order of 10^{-2} cm^2/Vs. The output characteristics (I_{DS}-V_{DS}) show current saturation as well as negligible contact resistance (see Fig. 2. for a α-sexithiophene based device).
In order to shed some light onto the possible mechanism causing stress, the temperature dependence of the drain current was measured with a continuous negative gate voltage applied to induce stress. A typical result is shown in Fig. 3. In

these experiments, the relaxed devices are first cooled down to 100 K without bias and then, while the drain current is being measured in the linear region they are heated to 320 K with a heating rate of 1.7 K/min.

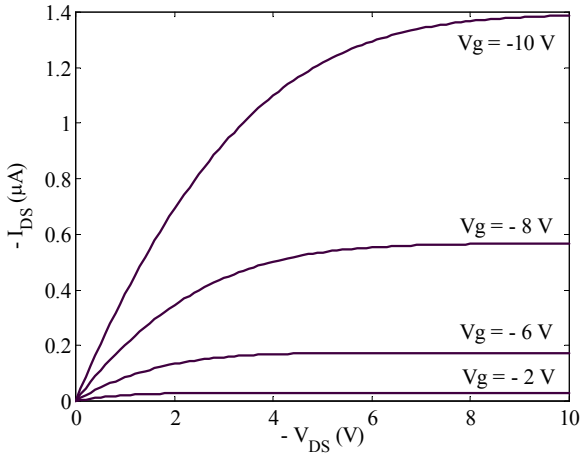

Fig. 2. Output characteristics of a α-sexithiophene (α-T6) transistor. Devices dimension are W/L =20000/10

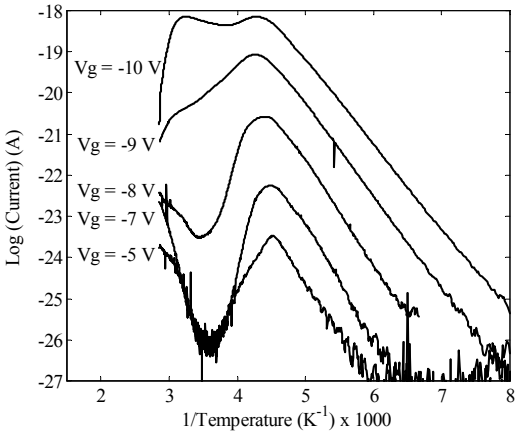

Fig. 3. Temperature dependence of the drain current showing the collapse in the current occurring at 220 K and near 300 K. Measurements done in the linear region (V_{DS} = –0.5 V) for a sexithiophene device.

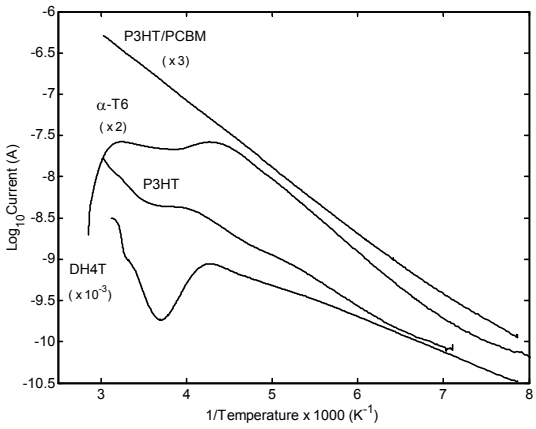

Fig. 4. Temperature dependence of the drain current measured in the linear region of different transistor devices based in different materials. The curves were shifted for clarity.

The drain current initially increases exponentially with the temperature, as expected. However, just before 200 K a change in the slope is noticeable. The current passes through a maximum at 220 K before decreasing with further rise in temperature to a minimum value occurring at 245 K. This decrease in current is caused by a continuous increase in the device threshold voltage. Therefore, we conclude that the stress-induced threshold voltage shift occurs only above 180 K. Below this temperature we observe that the threshold voltage does not depend on the gate bias stress.

In the temperature range [250–310 K] the current rises again suggesting that thermal activation of charge carriers is now dominating over the mechanism causing stress. Above 300 K the current decreases and stress effects take over, causing again a current collapse. These results show that there are two mechanisms involved in stress, or that the stress process has two components, which are likely to be related. It is interesting to note that each maximum is proceed by a shoulder, a similar behaviour has been observed in α-sexithiophene based transistors [8].

Stress effects were studied in a number of semiconductors such as DH4T, P3HT, and a mixture of two materials P3HT/PCBM. Fig. 4 compares the temperature dependence of drain-source currents for transistors based on different semiconductors. It is interesting to note that the current collapse near 220 K is common to the majority of the materials studied, despite the fact that they were processed in different ways. P3HT was deposited by spin-coating while the DH4T and the sexithiophene were deposited by vacuum sublimation. Striking is also the observation that a mixture of P3HT/PCBM is almost stable against stress effects

3.2 Thermal detrapping currents.

Physical properties of charge carrier traps in semiconductors are usually studied by thermally stimulated current (TSC) techniques. In TSC experiments the traps are filled with the bias when cooling down low temperature. Then, upon heating, the trapped carriers are released to the appropriate band and there is an increase in the free carrier density. The amount of trapped charge is finite, being limited by the number of traps, and as the temperature is increased further all the trapped carriers are eventually released. There is a peak in a plot of the current change as a function of temperature. The temperature at which this peak occurs is related to the energy level of the trap and the area under the peak is related to the trap concentration.

Charging of the traps was performed by application of a negative gate bias at a temperature of 320 K. Then, the transistor was cooled to 140 K, while keeping the stressing bias on. At low temperatures the bias was removed, the drain and source terminals connected to a picoammeter, and the device heated with a well-defined heating rate (typicaly between 1 and 3 K/mim). Figure 5 shows a TSC curve measured without trap filling (the device was cooled without a dc applied bias) and two curves with trap filling. Comparing Fig. 4 and Fig. 5, it is interesting to note that the onset of the thermal detrapping current coincides with the onset of stress (200-220 K). This suggests that the TSC peaks are related to the electronic process causing stress.

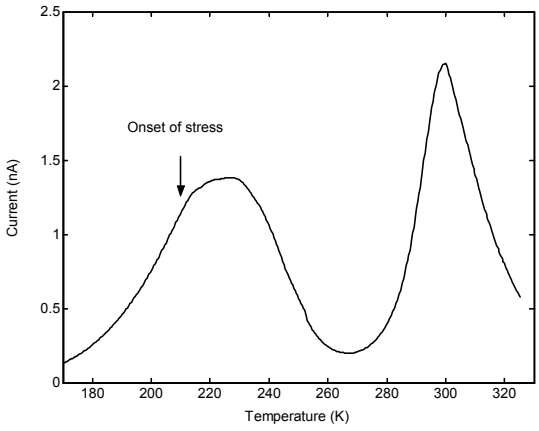

Fig. 4. Temperature dependence of the drain current showing the collapse in the current occurring at 220 K and near 300 K. Measurements done in the linear region (V_{DS} = –0.5 V and V_g = –12 V) for a sexithiophene device.

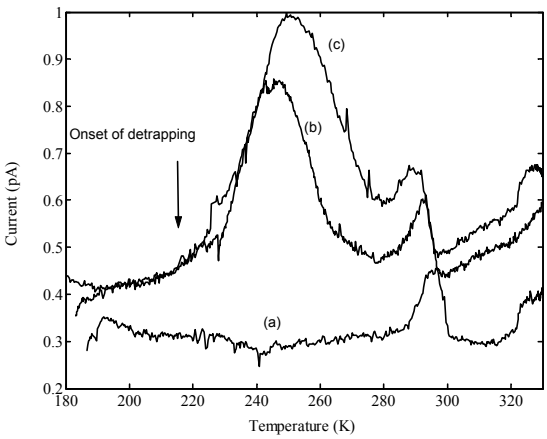

Fig. 5. Thermal detrapping curves measured at different heating rates and with different bias-filling conditions. (b) with a heating rate of 27.8 mK/s and (c) of 43.7 mK/s using a bias filling of –10 V. Curve (a) was recorded without bias-filling.

Unfortunately was not possible to extract quantitative information about the trap depth, because the peaks do not shift in a systematic form to higher temperatures with increasing heating rate. We believe this is due the fact that in transistors the TSC current is measured between two surface contacts (drain and source), channel conduction, recombination and re-trapping are expected to be important.

3.3 AC admittance measurements in MIS capacitors

The frequency response of an ideal MIS structure can be deduced from the equivalent circuit represented in Figure 1b. Here C_I represents the SiO_2 capacitance and C_D the depletion layer capacitance. The bulk semiconductor can be represented by the parallel combination C_B and R_B. The contact resistance is taken in account by R_C
This circuit has two relaxation frequencies, the main arising from the shunt of R_B on C_B and a high frequency relaxation frequency resulting from R_C, which it will not be considered here. The main device relaxation frequency will be given by

$$f_R = \frac{1}{2\pi R_B\left(C_D + C_B\right)} = \frac{1}{2\pi\tau} \qquad (1)$$

Where τ is the relaxation time of the device. Now for a MIS structure, R_B, C_B and C_D all vary with applied voltage through their dependences on the depletion region width, X_D, i.e.

$$R_B = \rho_S \frac{L - X_D}{A} \qquad (2)$$

$$C_B = \varepsilon_S \frac{A}{L - X_D} \qquad (3)$$

$$C_D = \varepsilon_S \frac{A}{X_D} \qquad (4)$$

Where A is the area of the device, L the thickness of the semiconductor organic layer and ρ_S and ε_S are, respectively, the resistivity and absolute permittivity of the semiconductor. Therefore, as the device is driven from accumulation (X_D=0) to full depletion (X_D=L) the relaxation frequency will change between the limits

$$\frac{1}{2\pi R_B^{'}\left(C_I + C_B^{'}\right)} < f_R < \frac{1}{2\pi\rho_S\varepsilon_S} \qquad (5)$$

Where R_B' and C_B' are the values of R_B and C_B when X_D=0 (accumulation regime).
The loss tangent or tan δ is plotted as function of frequency and temperature in Figure 6. As expected from equation 5, tan δ shifts to higher frequencies as the temperature rises. However, the behavior is not smooth; it is obvious that at 190 K occurs an abrupt change in the activation energy. Furthermore, above this temperature the peak amplitude starts to decreases with temperature. A second pronounced decrease in peak amplitude is visible at 245 K. This behavior is unusual because according to the equation 5 as the ionization of acceptor states increases with temperature the maximum values in tan δ should increase trough the dependence on R_B.
Summarizing, the temperature dependence of tan δ shows two major features, (i) a change in the activation energy and a (ii) a change in the accumulation capacitance. It is remarkable that these changes are abrupt and occurring at temperatures coincident with the changes observed in the transistor dc current (see Figure 4). In order to highlight this peculiar temperature dependence, in Figure 7 is represented the Arrenhius plot of the frequency position of the maximum value of tan δ and in Figure 8 it is plotted the temperature dependence of the maximum of tan δ.
The change in the activation energy implies a change in the bulk resistance R_B. Therefore, impedance measurements clearly show that gate-bias stress is affecting the bulk organic layer and not only the space charge layer near the dielectric/semiconductor interface. The decrease in the peak amplitude can be explained by a decrease in C_D. However any of the observations implies a change in the dielectric capacitance C_I.

It is also remarkable that a small ac field of 400 mV across the MIS capacitor is able to induce a pronounced stress effect. To our knowledge is the first time that stress effects in organic semiconductors are observed using ac impedance measurements.

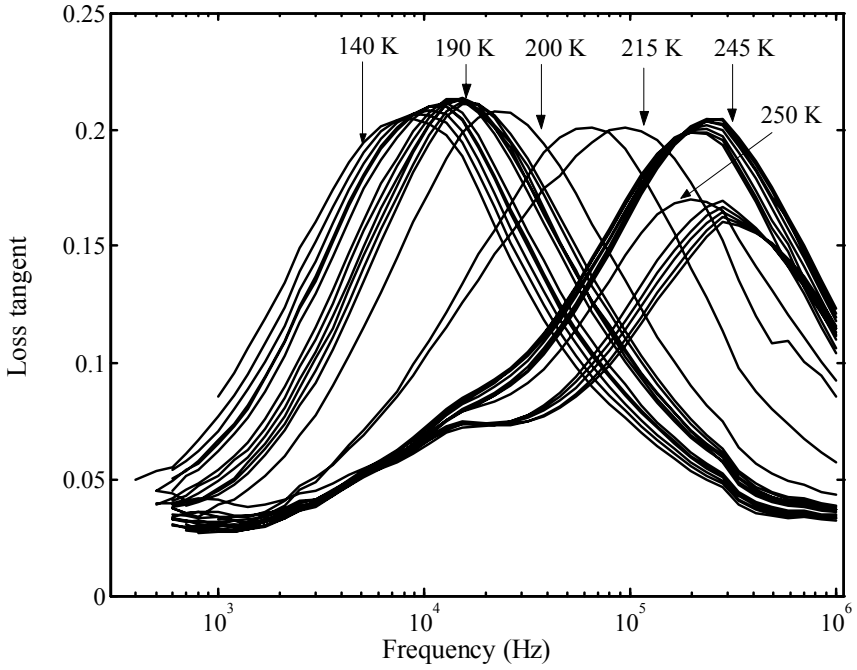

Fig. 6. Temperature dependence of the loss tangent.

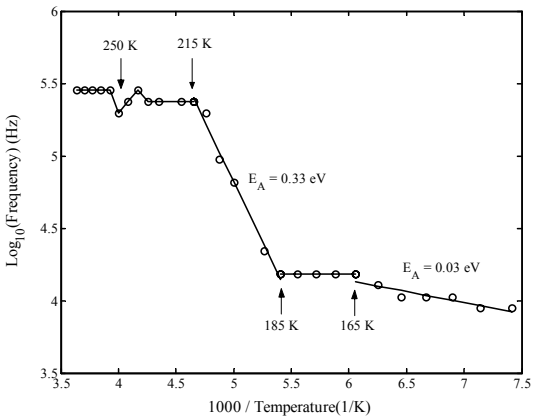

Fig. 7. Frequency position of the maximum in loss tangent as function of temperature.

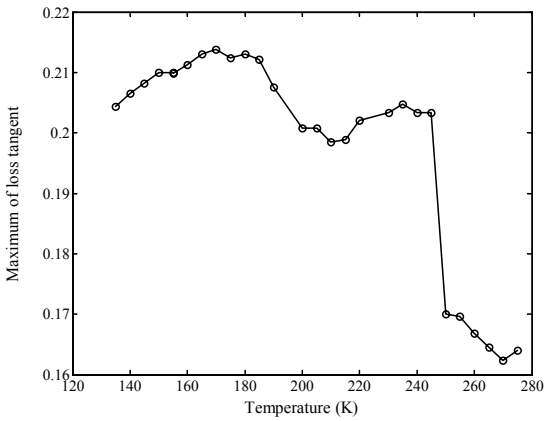

Fig. 8. Maximum of the loss tangent as function of temperature.

Capacitance voltage (*C-V*) measurements before and after stressing the MIS capacitor are shown in Fig. 9. It is clear from the figure that there is a shift toward higher negative voltages. The maximum capacitance in the accumulation region is an indication of the dielectric constant of the SiO_2 layer. It is evident from the *C-V* plots that there is no change in the dielectric capacitance. Therefore, we can now conclusively state that the change in the threshold voltage is solely due to defects in the organic semiconductor or at the dielectric/semiconductor interface.

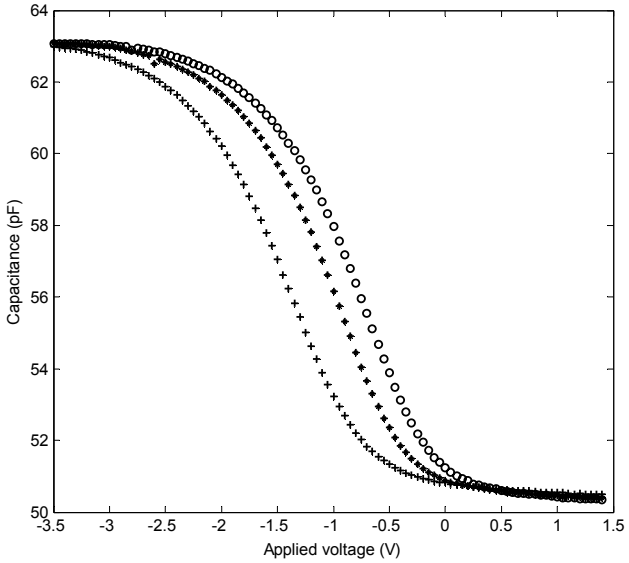

Fig. 9. Capacitance-voltage characteristics showing the effect of gate-voltage stress on a DH4T MIS capacitor. The three curves were recorded consecutively. (O) curve recorded without stress, (*) second curve recorded and (+) third curve recorded. Measurements were carried out using an ac signal of 400 mV with a frequency of 6 kHz.

4. CONCLUSIONS

In conclusion, thermal detrapping currents provide strong evidence that the gate-bias induced stress in organic based transistors, is due to trapping of charge carriers in the organic semiconductor. It is suggested that these traps have origin in a structural relaxation of the organic chain, occurring near 200 K for thiophene-based materials. This conclusion is supported by the observation that this relaxation is apparently independent of the thin film processing conditions and is observed in a variety of thiophene semiconductors. AC admittance measurements in MIS capacitors also support the view that the gate bias stress is intrinsic to the organic semiconductor.

Acknowledgements

The authors acknowledge financial support from the Portuguese Foundation for Science and Technology, project POCTI/FAT/47956/2002 and POCTI/CTM/41117/2001.

REFERENCES

1. A.R. Brown, C.P. Jarret, D.M. de Leeuw, and M. Matters, "Field-effect transistors made from solution-processed organic semiconductors", Synth. Met., **88**, 37-55, 1997.
2. M. Matters, D.M. de Leeuw, P.T. Herwig, and A.R. Brown, "Bias-stress induced instability of organic thin film transistors", Synth. Met., **102**, 998-999, 1999

3. S.J. Zilker, C. Detchverry, E. Cantatore, and D.M. de Leeuw, ”Bias stress in organic thin-film transistors and logic gates”, Appl. Phys. Lett., **79**, 1124 -1126, 2001.
4. W.A. Schoonveld, J.B. Oosting, J. Vrijmoeth and T.M. Klapwijk, “Charge trapping instabilities of sexithiophene thin film transistors”, Synth. Met., **101,** 608-609, 1999.
5. A. Salleo and R.A. Street, “Ligth-induced bias stress reversal in polyfluorene thin film transistors”, J. Appl. Phys, **94**, 471-479, 2003.
6. R.A. Street, A. Salleo, M. Chabinyc, “Bipolaron mechanism for bias-stress effects in polymer transistors”, Phys. Rev. B, **68,** 085316, 2003.
7. H.L. Gomes, P. Stallinga, F. Dinelli, M. Murgia, F. Biscarini, D.M. de Leeuw, T. Muck, J. Geurts, L.W. Molenkamp and V.Wagner, ”Bias-induced threshold voltages shifts in thin film organic transistors”, Appl. Phys. Lett., **84,** 3184-3186, 2004.
8. H. L. Gomes, P. Stallinga, F. Dinelli, M. Murgia, F. Biscarini, D. M. de Leeuw, M. Muccini and K. Mullen; “Electrical characterisation of organic based transistors: stability issues”; Polymers for Advanced technologies”, **16**, 227-231, 2005.