PAT

Electrical characterization of organic based transistors: stability issues[†]

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An investigation into the stability of metal insulator semiconductor (MIS) transistors based on α-sexithiophene is reported. In particular the kinetics of the threshold voltage shift upon application of a gate bias has been determined. The kinetics follow a stretched-hyperbola type behavior, in agreement with the formalism developed to explain metastability in amorphous–silicon thin film transistors. Using this model, quantification of device stability is possible. Temperature-dependent measurements show that there are two processes involved in the threshold voltage shift, one occurring at $T \approx 220\,K$ and the other at $T \approx 300\,K$. The latter process is found to be sample dependent. This suggests a relation between device stability and α-sexithiophene deposition parameters. Copyright © 2005 John Wiley & Sons, Ltd.

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INTRODUCTION

One of the most important stability issues in organic transistors is the shift in the threshold voltage upon applying a prolonged bias to the gate electrode, so-called stressing. The applied negative gate potential for a *p*-type semiconductor causes a build up of mobile charges at the semiconductor/insulator interface, which are then trapped. As a consequence, to reach an identical channel current subsequently, a higher gate voltage has to be used.

Devices suffering from gate-bias stress effects exhibit threshold voltage shifts ΔV_{th}, current-voltage characteristics with hysteresis and a slow and continuous decrease in the device current. These effects are particular noticeable when the negative gate bias is applied over prolonged time. Therefore, stress effects have a great impact on the application of organic semiconductors in electronic devices, e.g. limits the reliability of Thin Film Transistors (TFTs).

Bias stress effects are commonly observed in organic based TFTs. Stress has been reported for transistors based on pentacene, polythienylene vinylene (PTV),[1–3] α-sexithiophene,[4,5] poly-9,9′dioctyl-fluorene-co-bithiophene and regioregularpolythiophne.[6,7] In an attempt to understand the physical origin of this instability and the exact location of the trapped charges, several authors studied the effect using different dielectric materials,[1,3] different types of silicon oxide

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(SiO$_2$) as well as different surface treatments.[6] It is well established that ionic movements in thermally grown SiO$_2$ does not occur, therefore the data available in the literature suggest that stress in devices using thermally grown SiO$_2$ is related to the properties of the organic semiconductor itself. It is also known that the bias-stress effect is reversible and that the recovery process can be enhanced by a positive gate bias.[1,5] More recently it has been shown that stress can be also reversed by band gap light,[6] confirming the hypothesis that the phenomenon is due to charges trapped within the semiconductor film, near the dielectric interface. However, it still remains to be clarified why some organic semiconductors are more prone to this instability effect than others. Furthermore, even for the same material the bias-induced stress is apparent dependent on the device handling and processing.

Recently Salleo and Street *et al.*,[6] proposed that stress is due to the formation of less mobile bound hole pairs (bipolarons), the formation of these bipolaron states deplete the accumulation channel of mobile holes causing an increase in the threshold voltage. They based their conclusions on the observation that the decrease in the number of charge carrier is proportional to the square of their concentration. In the bipolaron mechanism the variations on the magnitude of the stress effects observed in different devices can then be explained as variations in the polaron binding energy from material to material. Furthermore the polaron binding energy can also be dependent on the structural disorder and impurities such as oxygen, making the device stability strongly dependent on the nature of the sample preparation.

If stress is an intrinsic property of the organic semiconductor, this suggests that some materials can be more suitable

than others to make TFTs. Therefore, when selecting organic molecules for TFTs applications, in addition to the usual considerations related with processing and charge carrier mobility values, the behavior against electrical induced stress should also be taken into account.

To study the effects of processing parameters or to compare electrical stability among different materials it is crucial to have a tool to quantify device stability. This problem has been addressed in the amorphous silicon (a-Si) technology for long time.[8–17] In a-Si TFTs it was found that the threshold voltage change ΔV_{th} induced by the application of a prolonged gate voltage can conveniently be modeled by a stretched exponential.[14,18,19,20] In this article it is shown that in organic based transistors the changes in V_{th} induced by stress also follows a stretched exponential behavior and therefore the models developed to quantify device stability in a-Si TFTs can, in principle, also be applied to organic transistors. The stability behavior of different organic semiconductors is also discussed.

EXPERIMENTAL

The α-T6 thin films (see chemical structure in Fig. 1) were deposited by thermal sublimation in a ultra-high vacuum organic molecular beam deposition apparatus (base pressure 10^{-9} mBar) onto pre-formed TFT test substrates, consisting of a heavily n-doped silicon gate electrode, a 200 nm thick (thermally grown) SiO_2 insulating layer ($C_{ox} = 19$ nFcm^{-2}) and a patterned gold layer as the source and drain electrodes. The channel dimensions were $W/L = 20\,000\,\mu m/10\,\mu m$. During the deposition, the sample substrate was held at 150°C. Gate bias stress has been carried out in the linear regime using $V_{DS} = -0.5$ V. The transfer characteristics were rapidly measured following a predetermined stressing time. All the measurements were carried out in vacuum (10^{-6} mBar). The transistors used in this study exhibit good characteristics, with a low off current, and a field-effect mobility of 1.7×10^{-2} cm^2/Vs. The I_{DS}–V_{DS} curves exhibit current saturation as well as negligible contact resistance.
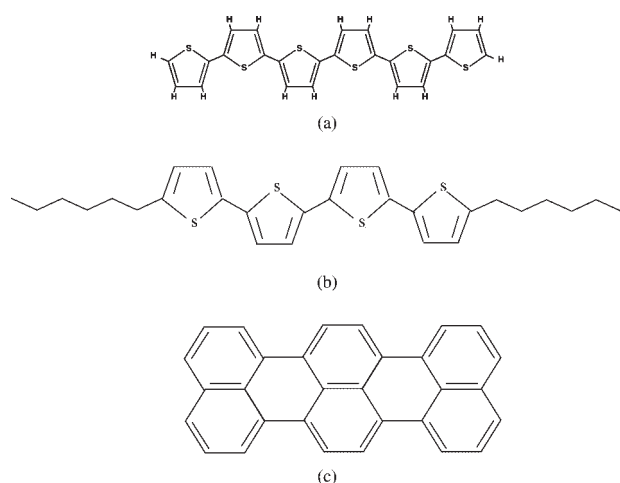

Figure 1. The molecular structure of same active materials used in this work: (a) sexithiophene, (b) dihexylquaterthiophene and (c) terrylene.

In all the stressing experiments described here, the devices are first heated to 340 K with a heating rate of 2 K/min while keeping a positive gate bias of 10 V applied. The devices are then brought to room temperature before the measurements were carried out. This procedure removes all the charges causing stress and therefore the device is in an unstressed initial state prior to the measurements.

The experimental data reported here is referred to sexithiophene based transistors, but other materials were also studied, such as dihexylquaterthiophene (DH4T) and terrylene (see chemical structures in Fig. 1). While sexithiophene and terrylene thin films were deposited by vacuum sublimation, DH4T is a soluble material deposited by spin coating.

RESULTS AND DISCUSSION

Theory

In this section, first the equations for a phenomenological description of the time dependence of the threshold-voltage shift (ΔV_{th}) are presented. It is assumed that the physical origin of ΔV_{th} is the creation of new electronic states or defects. The formalism allows us to quantify the device stability and is irrespective of the microscopic details of the process involved. For a-Si TFTs two major models were developed to explain V_{th} shifts.[12,13] Although, the underlying microscopic processes are different, in both models the creation of states is governed by a dispersive process, typical of amorphous materials. These models lead to a differential equation for the density of states created, ΔN_D, which is proportional to ΔV_{th}, since $\Delta N_D = C_{ox}\Delta V_{th}$. These states are the ones that must be filled before significant conduction can occur via accumulation layer. Thus, the more defects created during bias stress, the more holes are needed to occupy these defect states, resulting in a threshold voltage shift. In other words, the driving force for defect creation is charge trapping into defect-creation sites. Therefore, the rate at which defects are created depends on the density of free holes induced by the gate bias. In the course of gate bias stress, the free charge in the accumulation channel is replaced by charged defects. Based on these models it is readily shown that the rate of change in V_{th} is given by differential equation:[14,15]

$$\frac{dV_{th}}{dt} \propto \frac{d(\Delta N_D)}{dt} \propto N_{BT}(t)^\alpha \cdot \frac{t^{\beta-1}}{t_0^\beta} \tag{1}$$

where $N_{BT}(t)$ represents the concentration of free holes in the accumulation channel. Solving Eq. (1) with $\alpha = 1$ yields the stretched exponential function as given:

$$\Delta V_{th}(t) = \Delta V_0 \left\{ 1 - \exp\left[-\left(\frac{t}{\tau}\right)^\beta \right] \right\} \tag{2}$$

where ΔV_0 is the effective voltage drop across the insulator, k_B is the Boltzamann's constant, T is the temperature and β is a weakly temperature-dependent dispersion parameter. The time constant τ represents the characteristic trapping time of carriers. It is thermally activated according to:

$$\tau = \frac{1}{v_0} \exp\left(\frac{E_\tau}{k_B T}\right) \tag{3}$$

here E_τ is the mean activation energy that carriers need to overcome before they became trapped and v_0 is an attempt to escape frequency. By fitting the experimental data to a stretched exponential, one can extract the parameters β and τ. The E_τ value, for defect creation can thus be obtained by measuring the stretched exponential curves at different temperatures. According to Eq. (3), in a plot of the form $\log(\tau)$ as a function of $1/T$, the slope of this curve represents the activation energy, $E_\tau = E_a/\beta$, for defect creation. Therefore, the value of E_τ, is a measure of the device stability.

Several authors have reported deviations from the stretched-exponential, in particular for long stressing times ($t > 10^4$ sec) and wide temperature ranges. To account for this behavior an $\alpha > 1$ has to be introduced in Eq. (1). Solving for $\alpha > 1$ yields a modified form of the stretched exponential function. This function is also referred to as "stretched hyperbola".

Moreover, a formalism was then developed that combined the stress time t and temperature T in a so-called thermalization energy $E_{th} = k_B T \ln(vt)$ which can be interpreted as: all possible defect sites with $E_A \leq E_{th}$ have been filled at time t. According to this formalism, the time dependence of the threshold voltage shift can be described by the stretched hyperbola.[14,19,20]

$$\frac{V_{th} - V_{th}^{ini}}{V_g - V_{th}^{ini}} = 1 - \frac{1}{\left(\exp\left\{\frac{E_{th}-E_A}{k_B T_0}\right\} + 1\right)^{1/(\alpha-1)}} \quad (4)$$

where V_{th}^{ini}, is the initial threshold voltage and V_g the gate stress voltage. It has been claimed that this model provides a better description for the bias induced stress in a-Si TFTs over a wide range of stressing times and temperatures independently of the specific microscopic mechanisms involved.[18] In the stretched-hyperbola behavior, the parameter E_A corresponds to the most probable energy barrier for defect creation, the higher E_A the more stable is the device.

Experimental results

Figure 2 shows the evolution of typical experimental transfer characteristics after a negative gate bias stress, V_g, of -10 V for different stress times. The threshold voltage shifts to higher values and eventually the transistor channel will close. This effect arises from the accumulation of negative trapped charge that shields the external gate field.

Figure 3 shows, for a typical sample, the time dependence of the threshold voltage change during stressing and relaxation back towards its initial threshold voltage. As reported by others, the effect is reversible and can be enhanced if a positive gate voltage is applied.[5] The time dependence of these processes varies from device to device and it is related to device stability.

The variation of $\Delta V_{th}^{rel} = (V_{th} - V_{th}^{ini})/(V_g - V_{th}^{ini})$ with the stress temperature for different stress times is shown in Fig. 4. A constant gate bias stress of -10 V was applied for three different temperatures. The lines indicate fittings to a stretched exponential according to Eq. (2).

Although the fitting deteriorates in the extremes of the curves, the stretched exponential function can reasonably describe the experimental data.
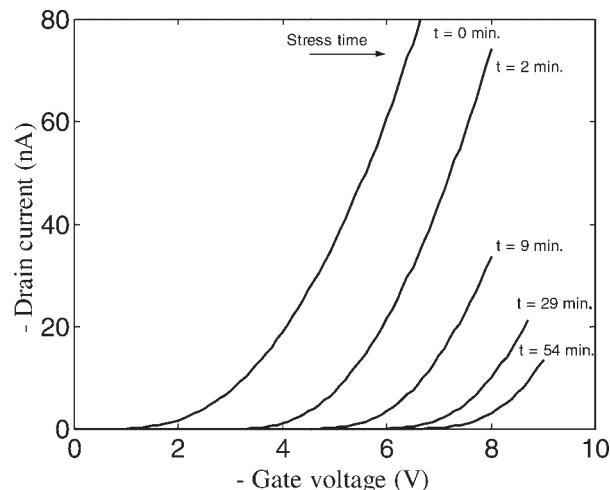
Figure 2. Evolution of the linear transfer curves with increasing stress time. The stressing voltage $V_g = -10$ V, and the curves were measured at $V_{DS} = -0.5$ V.
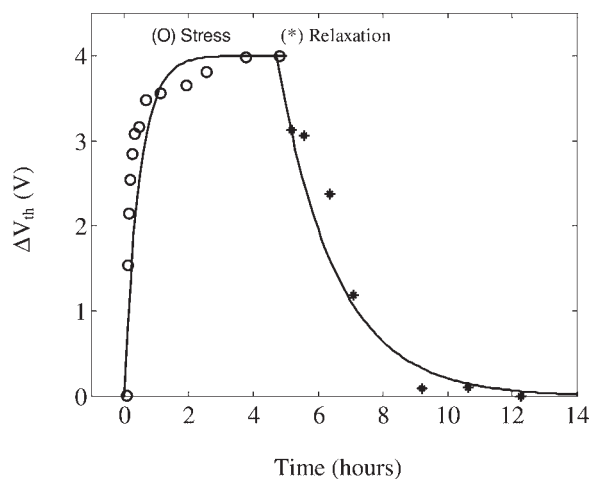

Figure 3. The evolution of the threshold voltage shift as function of time: (○) when stressing with a constant gate, (*) relaxing with $V_g = 0$ V.
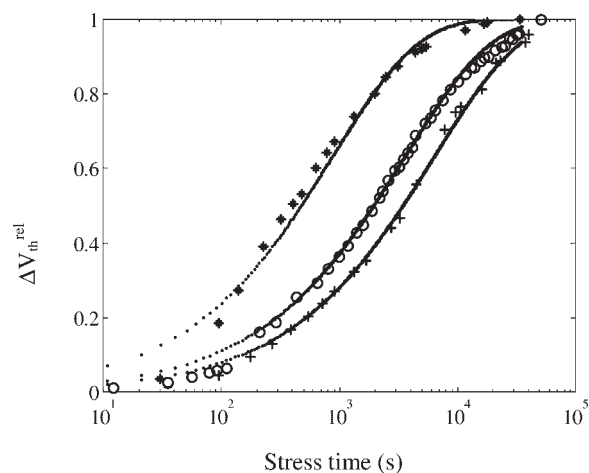

Figure 4. Relative threshold voltage ΔV_{th}^{rel} shift, versus stress time for fixed stress voltage (-10 V) and different stress temperatures. The symbols represent the data and the lines the fit to Eq. (1) using $\beta = 0.6$ and temperature dependent trapping time: (*) $\tau = 880$ sec., T = 320 K; (○), $\tau = 3600$ sec., T = 296 K; (+) $\tau = 6400$ sec., T = 290 K.
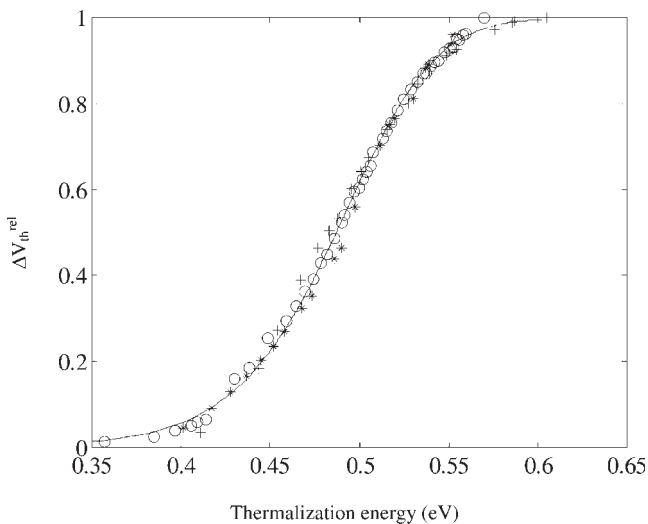
Figure 5. Measured values of relative threshold-voltage shift at 290 K (*), 296 K (○) and 320 K (+) plotted as a function of thermalization energy (see text for details). Also plotted (—) is the best fit curve based on Eq. (3).

Figure 6. Evolution of the subthreshold slope with stress time for a constant negative stressing voltage of 10 V.

The evolution of $\log \tau$, obtained from the fitting of the experimental data with Eq. (2), as a function of $1/T$ (results not shown) give an activation energy $E_\tau = E_A/\beta$ of 0.51 eV. According to the thermalization energy concept, the experimental curves recorded for different temperatures should fall on top of each other by selecting an appropriate attempt to escape frequency v. Figure 5 shows the relative threshold voltage shift ΔV_{th}^{rel} as a function of the thermalization energy. The curves recorded at the temperatures of 290, 296 and 320 K will overlap only if a frequency of about 10^5 Hz is used. For fitting the data points (Fig. 5) the stretched-hyperbola formalism of Eq. (4) was used, $\alpha = 1.5$ and $v = 10^5$ Hz. The only fitting parameters were E_A and $k_B T_0$, which were systematically changed to yield the best fit to the data. From the fitting the values obtained were $E_A = 0.52$ eV and $k_B T_0 = 33$ meV.

This activation energy is identical to the one obtained using the stretched exponential fitting in Fig. 4. It is interesting to note that the value of $E_A = 0.52$ eV for defect creation obtained using the stretched exponential or stretched hyperbola formalism is surprisingly equal to the value estimated by Salleo and Street[6] for the polaron binding energy.

It has been often reported that gate-bias induced stress does not affect the charge carrier mobility. This is readily confirmed by the observation that the transistor transfer curves shift in a parallel fashion. However, assuming that stress can be related to trap states located near the semiconductor/insulator interface, one expects that stress should then affect the subthreshold slope. In the subthreshold region, the Fermi level sweeps the bandgap and, thus, the TFT characteristics are very sensitive to traps in the active layer. Figure 6 shows the transfer curves for a device when stressed with a gate voltage of −10 V. At certain times the stress was interrupted and a transfer curve was recorded. As clearly seen in Fig. 6, in the subthreshold region the transfer characteristic are parallel.

In order to shed some light onto the possible mechanism causing the stress, the temperature dependence of the drain
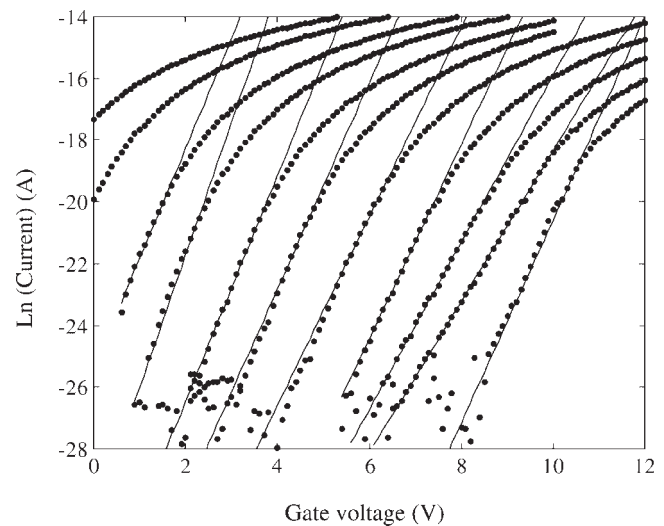
current was also measured. In these experiments the devices are first cooled down to 100 K and then while the drain current is being measured they are heated to 340 K with a heating rate of 2.4 K/min.

The temperature dependence of the drain current for two different devices (A and B) is shown in Fig. 7. For both devices the drain current initially increases with the temperature, as expected. However, at approximately 220 K the current passes through a maximum before decreasing with further increase in temperature. This anomalous decrease in current is caused by a continuous rise in the device threshold voltage. Therefore, it is concluded that the stress-induced instability in threshold voltage occurs only above 220 K. Below this temperature it was observed that the threshold voltage is stable and insensitive to gate-voltage stressing.

For temperatures below 250 K all the devices show a similar behavior, however as the temperature approaches
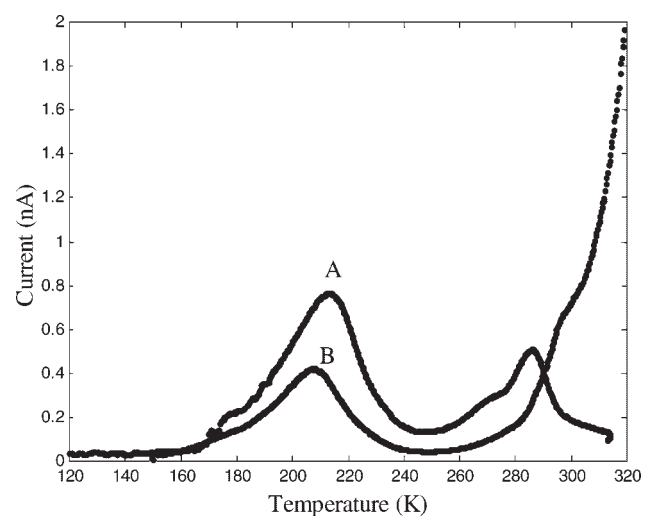

Figure 7. Temperature dependence of the drain current recorded in two different devices, named A and B. Measurements done in the saturation region ($V_{DS} = -10$ V and $V_g = -10$ V).

300 K significant variations can be observed for devices belonging to different batches. While some devices show a second peak, others exhibit a continuous rise in current that dominates over the stress effect. Figure 7 shows these differences for two devices named A and B. The presence of a shoulder at 300 K in curve B indicates that the second peak is still present, but now it is hidden below a stronger thermal activation of the current. Therefore, the magnitude of the bias stress effect is smaller in device B compared to device A, when measured at room temperature.

This result suggests that device sensitivity to stress is related to device processing parameters or sample handling.

It is clear that there are two major processes causing bias-induced stress; one located between 200 K and 250 K and the other occurring around 300 K. In between, stress competes with the current rise due to thermal activation. It is also interesting to note that each maximum shown in Fig. 8 is preceded by a small shoulder indicating rather complex temperature dependence.

Stress effects were also studied in DH4T and in terrylene based transistors. While DH4T exhibit pronounced stress effects in a similar way as observed in sexithiophene,[21] no signs of gate-bias induced instabilities were detected in terrylene-based transistors. This observation raises an important question: is the device electrical stability related to the semiconductor molecular structure?

Terrylene is a three-unit oligomer of poly(peri-naphthalene). The molecular structure is intermediate between polyacetylene and graphite (see Fig. 1). This fused ring structure is more rigid than sexithiophene and DH4T and evades ring-rotation known to be an obstacle to π-conjugation and also inhibits Peierls distortion through bond length alternation by inclusion of all CC bonds in aromatic rings. Thus, the susceptibility to local distortions upon charging can be reduced. In other words the formation of double charged bipolaron states is unlikely. Therefore, the absence of electrical induced stress in terrylene based transistors seems to supports the bipolaron mechanism proposed by Street *et al.*[7] In this model the stress is caused by the formation of double charged hole states (bipolarons). The terrylene rigid molecular structure prevents structural relaxation associated to polarons, therefore, the high stability can then be due to a low polaron binding energy.

CONCLUSIONS

In conclusion, it has been shown that a phenomenological description used in studies of stability in a-Si TFTs is applicable to organic based transistors. Using this description, physical meaningful parameters are extracted that can be used as an indication of the device stability. Using this formalism a defect creation energy of $E_A \approx 0.52\,eV$ is obtained for sexithiophene based devices. This result agrees well with the estimated bipolaron binding energy as reported by Salleo and Street.[6] Furthermore, the absence of gate–bias induced stress in terrylene based transistors seems to support that stress is caused by the formation of charged polarons.

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