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Switching in polymeric resistance random-access memories (RRAMS)

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Abstract

Resistive switching in aluminum-polymer-based diodes has been investigated using small signal impedance measurements. It is shown that switching is a two-step process. In the first step, the device remains highly resistive but the low frequency capacitance increases by orders of magnitude. In the second step, resistive switching takes place. A tentative model is presented that can account for the observed behavior. The impedance analysis shows that the device does not behave homogenously over the entire electrode area and only a fraction of the device area gives rise to switching.
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1. Introduction

Electrically switchable solid state memories have been demonstrated in diodes using a variety of organic materials. The key feature of these memories is the ability to switch their resistance between two or more stable states simply by applying voltage pulses. Many devices exhibit sufficiently fast switching capability, low switching threshold voltages giving ON/OFF current ratios up to 10^6 and long retention times, thus opening interesting perspectives for applications in the domain of resistance random access memories (RRAMs).

Several memory architectures have been reported. Bistable organic diodes made of a single organic layer between two metal electrodes [1–17], nanoparticles embedded into an organic matrix [18–21], organic layers with granular metals [22–25] and transistor type memories [26,27].

We also reported bistable resistance characteristics in metal/polymer/metal diodes [28]. We showed

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that the current is transported through filaments and that the formation of a thin aluminum oxide layer was crucial for the fabrication of reliable switching devices. Multi-level stages can be obtained depending on the number of filaments. Recently, our findings were corroborated by Karthäuser and co-workers [29] who elegantly showed that switching characteristics can be obtained simply by depositing an aluminum film directly onto the substrate and without the need for an organic layer. Previously, Oyamada et al. [12] had also concluded that the aluminum electrode is responsible for electrical switching. As long ago as 1990, Sato et al. [30] proposed that the contact between the aluminum and the semiconductor plays an essential role. This inference was supported by the experimental fact that no observable switching effect could be found when other electrode metals such as nickel or gold were employed instead of aluminum. Similar results were reported by Beck et al. [31].

In practice, since the memory effect seems intimately related to the presence of oxide, the switching in binary oxides and perovskite-type oxides is clearly relevant. In these materials switching is attributed to deep trapping processes. For instance, trapped charges in nanometer-thin insulating layers of Al_2O_3 were reported to exhibit a remarkable resistance to annihilation by opposite polarity carriers passing through the oxide [32]. Retention times are estimated to be as long as 10 years [33].

Much knowledge about carrier trapping in interfacial oxide layers in a variety of devices has been provided by small signal impedance spectroscopy. It is thus surprising that detailed studies of the impedance characteristics in switching devices have not been conducted. The scarce reports [30,34,35] do, however, show a behavior common to all memory device architectures: the switching is always accompanied by an increase in the device capacitance at low frequencies and explained as a trapping process. Simon et al. [36] have been shown that the trapped charge gives rise to inductive effects. Another study interpreted the impedance data in terms of different density of highly conducting molecules [37]. Here, we report a systematic and detailed analysis of the impedance changes occurring in the devices as they are formed and subsequently programmed into high conductance states. We show that prior to resistive switching, the device undergoes a dramatic increase in the capacitance. In spite of this change, the device still behaves as an insulator and no appreciable dc currents can be measured. Switching to higher conducting levels can then be triggered by a subsequent voltage pulse.

The frequency dependence of the admittance reveals that the observed changes are located at the aluminum/polymer interface. The initial capacitance change is caused by a trap filling mechanism occurring at the aluminium/polymer interface. These traps were likely created in a previous process, the so-called "forming", a term first used by Simmons and Verderber [38] in 1967. Since then, the term "forming" has been used by a number of authors to describe a permanent change in the oxide, induced by a once-only voltage or current pulse in oxide-based memories [39–42]. Memory switching can only be initiated after this forming stage. The results described in this contribution were on devices that had already been formed.

2. Experimental

The structure of the electrically-bistable device studied here and the schematic flat-band diagram are presented in Fig. 1. The polymer used as the active layer was poly(spirofluorene) (PFO) for which the electron affinity, $\chi = 2.2$ eV, ionization potential, $I_p = 5.1$ eV and energy gap, $E_g = 2.9$ eV [16]. The aluminium (Al) and barium (Ba) electrodes have workfunctions $\phi_{Al} = 4.3$ eV and

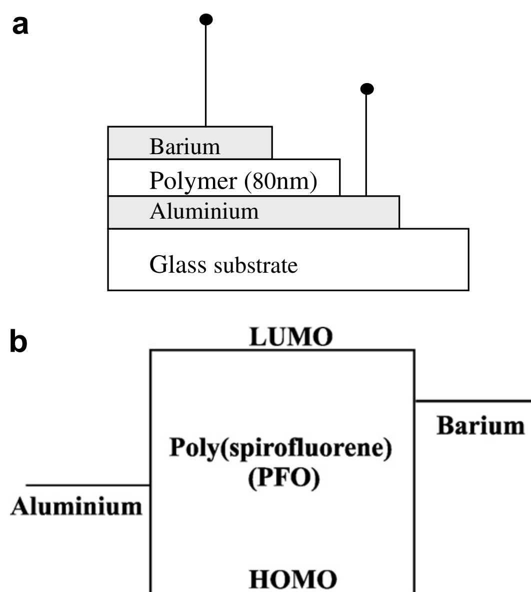

Fig. 1. Schematic diagram showing: (a) the physical structure of the memory device (top electrode is Ba, Al) and (b) the energy levels of the structure.

$\phi_{Ba} = 2.7$ eV, respectively. The methods used for fabrication of these electron-only diodes were described in Ref. [28]. The polymer thickness was 80 nm and both metal electrodes were 30 nm thick. The top electrode is 5 nm Ba with 100 nm Al. Effective device areas were either 0.01 or 0.09 cm^2. The aluminum electrode was treated with UV/O_3 plasma treatment before polymer deposition. The current–voltage (*I*–*V*) curves were obtained using a Keithley 487 picoammeter/voltage source and capacitance–frequency and capacitance–voltage (*C*–*V*) curves were obtained using a Fluke PM 6306 RLC meter. In all the measurements, voltages are referenced such that the Ba/Al electrode is held at local ground, while the bias is applied to the Al electrode.

3. Results and discussion

3.1. Current–voltage characteristics

Fig. 2 shows typical current–voltage (*I*–*V*) characteristics obtained for two programmed states. The lower *I*–*V* curve corresponds to the "OFF state" and the higher curve to what we designate the "fully-ON state". In between, multilevel stages can be observed, see Ref. [28]. The different conductive states can be programmed by application of a voltage pulse, for example 3–5 V for 5 s. The process is totally electrically reversible, as described previously [28]. In the OFF state, the *I*–*V* curves can sometimes exhibit rectification properties as in Fig. 2. Current–voltage characteristics corresponding to the OFF state frequently show a shoulder at low positive bias at about the built-in voltage (see Fig. 2). This plateau/shoulder has often been observed in polymeric light emitting diodes (PLEDs) and will be discussed later when treating the capacitance–voltage (*C*–*V*) characteristics.

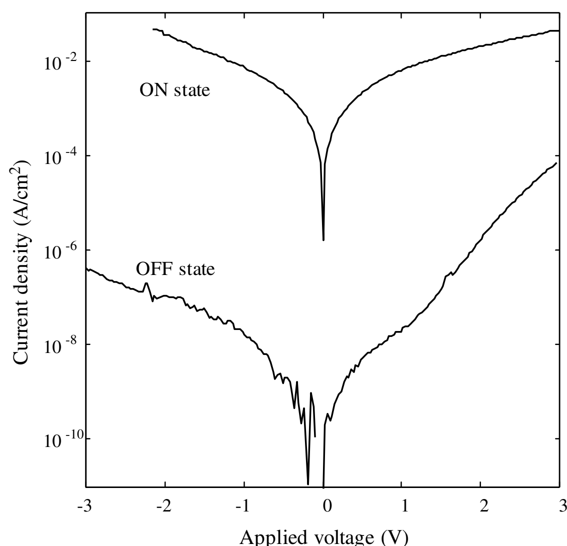

Fig. 2. Typical current density vs. voltage characteristics of an Al/ polyspirofluorene/BaAl device. The lower curve corresponds to the OFF state and the upper curve to a high ON state. The switch between the states is done by an external voltage pulse.

3.2. Small signal impedance characteristics

The OFF state and the ON-state observed in the *I*–*V* characteristics are associated with corresponding changes in the impedance characteristics. However, the changes do not occur simultaneously, capacitance changes precede changes in the current–voltage characteristics.

The changes occurring in the frequency-dependence of the admittance of devices in the OFF and ON states is shown in Fig. 3a. When the devices are OFF they behave as simple parallel plate capacitors with capacitance (*C*) and dielectric loss (G/ω) almost independent of frequency (*f*), where *G* is the conductance and $\omega = 2\pi f$, is the angular frequency. As no free carriers are able to follow the modulation of the external voltage at high frequencies, the material system behaves like a passive dielectric medium.

If the devices are submitted to voltage ramps (0.1 V/s) within a small range (e.g. ±5 V) a dramatic increase in capacitance at low frequencies may be induced. The rise in capacitance is accompanied by the appearance of a relaxation process with a cut-off frequency near 200 kHz, see Fig. 3a.

In this work, we chose to induce the capacitance change by cycling a triangular voltage ramp from 0 V to 5 V to 0 V with a scan speed of 0.1 V/s until the change was observed. We found this procedure more reliable than applying a voltage pulse, which can also induce the state. However, a voltage pulse frequently also induces resistive changes. The several device stages can also be observed when the device is switching from full ON to OFF states. However, we have not found a procedure to address the different states in a controllable way.

The OFF state also shows evidence of a weak relaxation frequency occurring near 1 MHz as shown in Fig. 3a. The high frequency dispersion here is likely to be caused by a small contact resistance. Once the device is triggered to the high capacitive state the associated relaxation, which occurs at

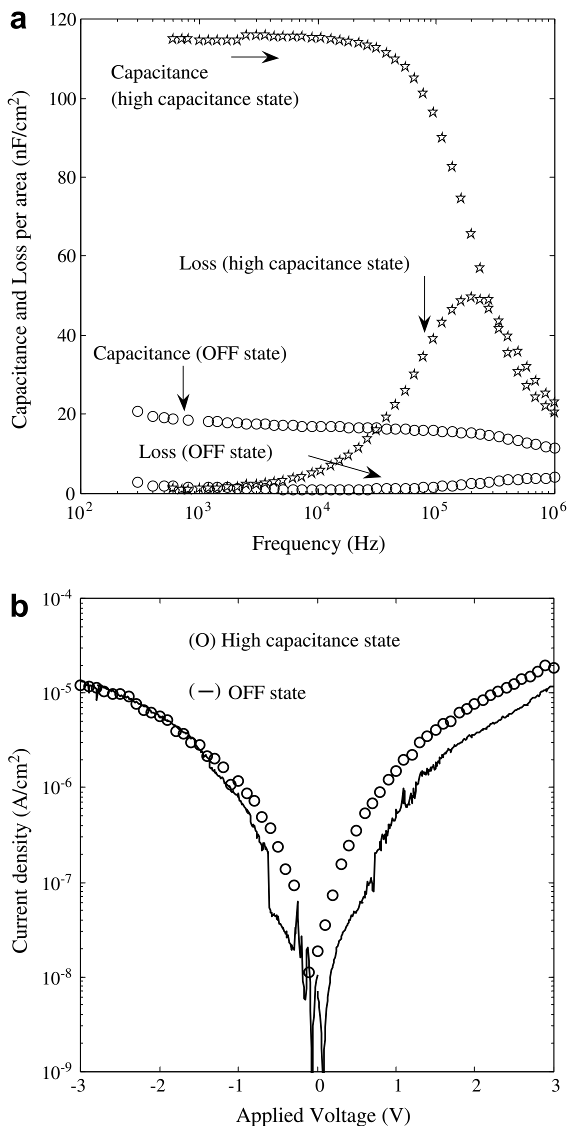

Fig. 3. (a) Frequency dependence of the measured capacitance (C) and the loss (G/ω) for an OFF state and for a high capacitance state. (b) The corresponding current voltage characteristics.

200 kHz, completely swamps the relaxation due to contact effects.

Crucially, the increase in device capacitance does not cause major changes in the current–voltage characteristics as shown in Fig. 3b. While there is some evidence for partial switching above about $\pm$0.5 V, the device is still considered to be in a low-conductance OFF state even though the currents are higher than in Fig. 2. This is further confirmed by the low-frequency (<1 kHz) behaviour of the loss curves for both the OFF and high capacitance states. At low frequencies, the DC resistance, R_{DC} of the device contributes a component, $1/2\pi R_{DC}$, to the overall loss. As seen in Fig. 3a, despite a major change in capacitance (from $\sim$20 to $\sim$120 nF/cm^2) the loss curves simply merge together as the frequency decreases with only a slight increase to $\sim$3.6 nF/cm^2 observed at $\sim$300 Hz. Attributing this to the DC leakage through the device we estimate R_{DC} to be $\sim$14.6 MΩ. The capacitance increase is thus a process that occurs prior to the onset of significant switching. Later, we will show that when the samples are programmed to high conductance states this is always accompanied by an increase in the low frequency loss (G/ω).

Once the device is in the high capacitance state, it can switch to higher conductive states (multi-level states) by applying a voltage pulse (typically 5–11 V for 5 s). Changes are now observed both in the current–voltage characteristics and in the ac conductance while the low-frequency capacitance remains constant. This behavior is seen in Fig. 4 where the capacitance (C) and loss (G/ω) for two ON states are presented. The higher conductive state yields a higher loss at low frequencies which rises as $1/f$ as expected for a dc resistance. The changes in the device are now purely resistive. The dispersion centered on 200 kHz is typical of the Maxwell–Wagner relaxation process [43] observed in two-layer dielectric structures and can

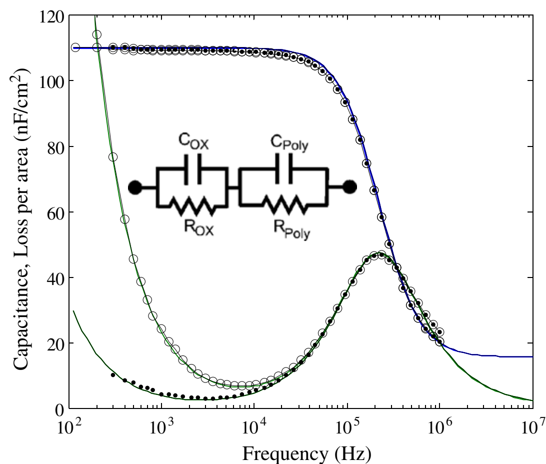

Fig. 4. Experimentally measured admittance (points) and theoretical fits (continuous lines) for two multi-level ON states using the equivalent circuit in the inset. The fitting parameters are shown in Table 1. The changes are purely resistive and only located in the high capacitive layer of the sample; only R_{OX} changes.

be modeled, therefore, by the double RC circuit in the inset of Fig. 4. This circuit exhibits dispersion in capacitance centered around a relaxation frequency, f_R, given by

$$f_R = \frac{1/R_{\mathrm{POLY}} + 1/R_{\mathrm{OX}}}{2\pi(C_{\mathrm{POLY}} + C_{\mathrm{OX}})}, \tag{1}$$

which for $R_{\mathrm{OX}} \gg R_{\mathrm{POLY}}$ reduces to

$$f_R = \frac{1}{2\pi R_{\mathrm{POLY}}(C_{\mathrm{POLY}} + C_{\mathrm{OX}})}. \tag{2}$$

In this case it is seen that f_R is sensitive to R_{POLY} and will move to higher frequencies as R_{POLY} decreases.

Without discussing, for the moment, the physical origin of the components in the circuit, we use this conceptual model to fit the experimental data in Fig. 4. The fitting parameters are shown in Table 1, from which it can readily be seen that the changes are purely resistive and only located in the high capacitive layer of the sample; only a decrease in R_{OX} from 500 MΩ/cm^2 to 70 MΩ/cm^2 is required to provide a good fit to the data. As can be seen, the relaxation frequency of the main dispersion (controlled essentially by R_{POLY}) is unaffected.

The electrical characteristics described up to now are typical for devices in the ON state with current densities in the order of 10 mA/cm^2. However, devices programmed to higher conductances, with current densities in the order of 0.1–1.0 A/cm^2 exhibit a different low frequency impedance response as shown in Fig. 5. The capacitance now increases rapidly with decreasing frequency. However, this increase is accompanied by a reduction in the capacitance in the previously constant capacitance region below the relaxation frequency. These effects are not yet clearly understood; we assume that they are related to the high currents passing through the device.

Table 1
Parameter values used to fit the experimental capacitance (C) and loss (G/ω) curves shown in Fig. 4

Circuit elements	C_{OX} (nF/cm^2)	R_{OX} (MΩ/cm^2)	C_{POLY} (nF/cm^2)	R_{POLY} (kΩ/cm^2)
State ON (a)	110	500	18	56
State ON (b)	110	70	18	56
State OFF	≫18	>2000	18	≫1000

Also given for comparison are the capacitance and resistance corresponding to the OFF state as shown in Fig. 3a. In the OFF state in Fig. 3a, however, since $f_R \ll 100$ Hz, then R_{POLY} must be ≫1000 kΩ and that C is dominated by C_{POLY} which is much less than C_{OX}.

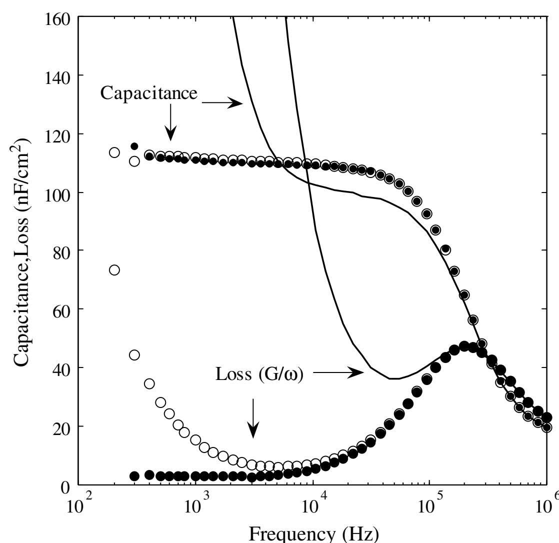

Fig. 5. The capacitance behavior when the device is programmed into very high conducting states. These states exhibit very high loss at low frequencies.

In summary, there are two major steps in the switching behavior as observed in the device admittance characteristics:

(a) *Capacitive switching:*
Capacitance switching is the first step. It has a signature in the capacitance but goes unnoticed in the I–V characteristics. The frequency response of the admittance shows that the device undergoes a change from a pure, capacitor-like behavior to a double-layer structure behavior following a significant reduction in the polymer resistance.

(b) *Resistive switching:*
Once the capacitive state is induced, the device can be programmed to a number of multi-level ON-states using voltage pulses of increasing magnitude. The changes in admittance are now purely resistive. Simulations using the equivalent circuit approach confirm that the resistive changes occur only in the high capacitance layer of the device.

3.3. Capacitance–voltage characteristics

Switched devices also exhibit three different types of C–V plots corresponding to the three different states of the sample, i.e. the OFF state, the capacitive

state and multi level ON-states. In the OFF state, the device capacitance exhibited a voltage-independent capacitance (not shown) confirming that, in this state, the device behaves as a pure capacitor. In the multi-level ON-states, the capacitance has a maximum at zero bias which decreases for both positive and negative applied bias. Such behavior is seen in Fig. 6. The AC conductance–voltage plot in the inset shows that the device exhibits a high conductance which depends symmetrically on applied voltage. The decrease in capacitance with increasing bias in the ON state is likely to be caused by the collapse of the oxide resistance shunting the capacitance as the bias increases.

Often when the device has suffered a capacitive switching but is still in the OFF state, the C–V plot can also show anomalous behavior, see Fig. 7. Here, the capacitance decreases at ~1 V but then increases sharply for increasing positive voltage above 2 V. When this bias dependence is observed the corresponding I–V characteristics exhibit a shoulder or a knee as observed in Fig. 2. The dip in the C–V plot and the shoulder in the I–V curve both occur at a similar voltage (between 1 and 2 V) suggesting that they are correlated. Such behavior is only observed when the device rectifies as the conductance curve in the inset of Fig. 7 (recorded simultaneously with the C–V plot) clearly shows.

Inductive dips in C–V plots have often been reported in the literature of inorganic based devices and recently for polymeric light emitting diodes, where even negative capacitances have been reported [44–48]. In PLEDs, the observation of negative differential capacitance has been attributed to space-charge limited transport [49,50], but in a similar way, it can also be explained by inductive effects due to minority carriers. The underlying physics has been well described by Misawa for pn junctions [51] and by Green and Shewchun for Schottky barriers [52] and MIS tunneling diodes [53]. When the current is minority-carrier dominated and the frequency is high, the current cannot follow the voltage instantaneously; the current starts lagging behind the voltage and a shift of the phase of the current relative to the voltage occurs. If the phase shift is large, this effect can even imitate negative capacitance. It must be noted that this is not a true capacitance in the sense that the device can store charge, but is rather an as-measured capacitance caused by a phase shift of the ac current. The important aspect of this behavior is that it is expected to occur when a thin insulating interfacial layer or a dipole layer exists between the electrode and the semiconductor.

Since there are no depletion layers in the device, the increase of capacitance after the dip deserves some comment. In forward bias, above the dip in the C–V plot, both the majority and minority carri-

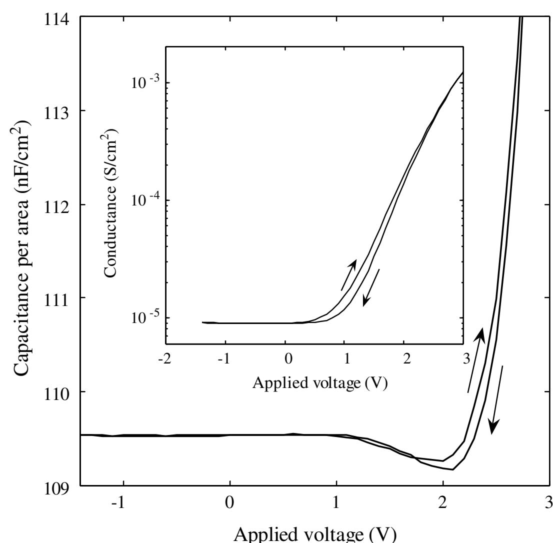

Fig. 7. Capacitance–voltage characteristic showing an inductive dip. The inset shows that this behavior is accompanied by a rectifying conductance–voltage curve. The conductance was recorded simultaneously with the capacitance at a frequency of 900 Hz.

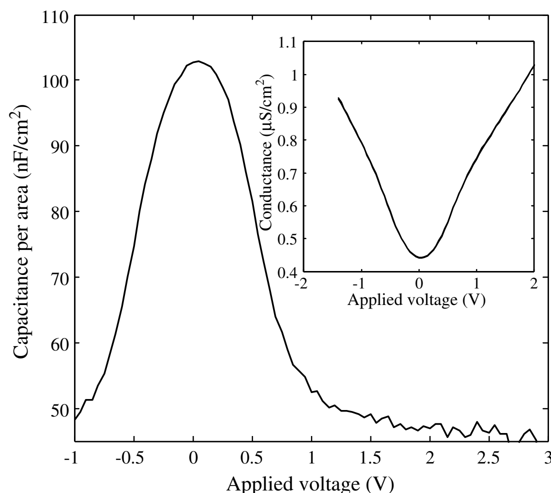

Fig. 6. Capacitance–voltage curve recorded when the sample is in the ON state. The conductance vs. voltage plot is represented in the inset showing that the device has a high and symmetrical conductance–voltage characteristic. The measurements were recorded at a frequency of 100 Hz.

ers contribute to the total device current. But the minority carriers are still a significant fraction of the total current. This minority carrier density will give rise to a diffusion capacitance. This contribution to the device capacitance increases with the applied bias in a similar way to the diffusion capacitance increase in a pn junction after the collapse of the depletion layer [54,55].

3.4. Phenomenological model

3.4.1. Capacitive switching

In this section, we propose a tentative model to explain the admittance data. Supported by the results discussed earlier, we assume that there is a thin oxide layer at the aluminum electrode. In the OFF state, the resistances of both the oxide and the polymer are high so that the AC equivalent circuit of the device reduces to two ideal capacitors in series and may be represented by the band diagram in Fig. 8a. As expected, the device capacitance displays a nearly flat frequency response. The weak dispersion appearing near 1 MHz in Fig. 3a we attribute to a resistance arising from the contacts and interconnecting tracks and cables in series with the geometric capacitance.

Under bias stress, either from the direct application of a pre-set voltage or from voltage cycling, the oxide layer undergoes an irreversible migration of atomic species, a process known in the literature as "forming". We suggest that this forming process creates hole traps in the oxide or at the polymer/oxide interface. As long as the traps are unfilled, the barrier for conduction through the oxide is high and the device remains in the low conductance OFF state.

When positive bias is applied to this electron only device, electrons injected from the Ba electrode drift through the polymer and accumulate at the polymer/oxide interface (Fig. 8b). Several consequences now follow: (i) the field across the oxide increases, thus encouraging hole (minority carrier) injection from the aluminum electrode into the oxide where most become trapped while the remainder are injected into the polymer, (ii) the presence of extrinsic charge carriers, both electrons and holes, in the polymer reduces its resistance and (iii) hole trapping in the oxide encourages further accumulation of electrons at the interface, creating a dipole layer of increasing polarization.

As the concentration of extrinsic carriers in the polymer increases, R_{POLY} becomes sufficiently low to shunt C_{POLY} giving rise to the large increase in low-frequency capacitance (capacitance switching) and the frequency dispersion seen in Fig. 3a.

3.4.2. Non-uniform switching

Assuming that the changes described above occur uniformly over the diode area and that

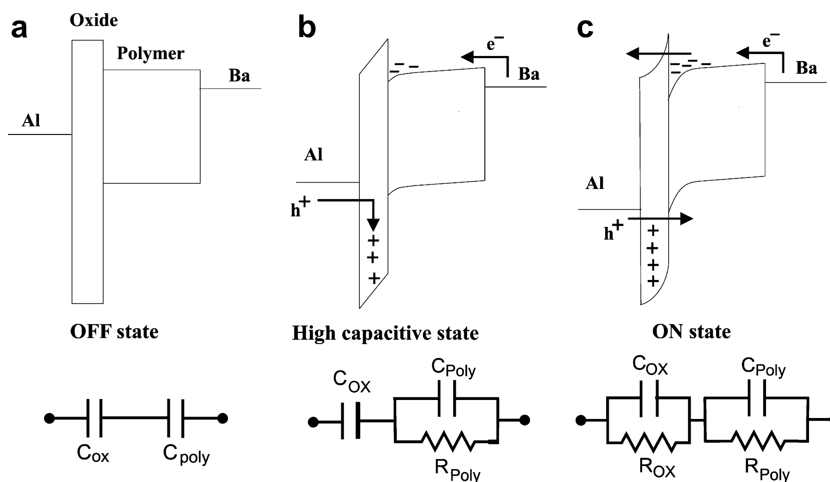

Fig. 8. Energy-band diagram (not to scale) and the respective equivalent circuit model as the device switches from an OFF state to a higher conductive state. (a) Equilibrium band diagram, the AC equivalent circuit of the device reduces to two ideal capacitors. (b) When positive bias is applied electrons injected from the Ba electrode drift through the polymer and accumulate at the polymer/oxide interface. R_{POLY} becomes sufficiently low to shunt C_{POLY} giving rise to the large increase in low-frequency capacitance (capacitance switching) and the frequency dispersion. (c) Higher voltages lead to increased electrical stress across the oxide reducing the oxide resistance R_{OX}, which is the current limiting layer controlling the low-frequency loss in Figs. 3a and 5 following capacitive switching.

$R_{POLY} \ll R_{OX}$, then the low frequency capacitance should increase to >600 nF/cm^2, consistent with an oxide layer <10 nm thick. However, the measured low-frequency capacitance at ~110 nF/cm^2 is much lower.

From the *I–V* plots in Fig. 3b we note that capacitance switching is accompanied by a small but significant increase in DC current through the device, suggesting that R_{OX} decreases as well as R_{POLY}. Such a decrease may be anticipated as the trapped hole and accumulated electron concentrations both increase. Fields in the oxide become highly non-linear, modifying the band diagram as shown in Fig. 8c so that interface conditions are conducive for electron tunneling from the polymer into the oxide, thus reducing R_{OX}. Therefore, we must now consider the full expression for the low-frequency capacitance of the device, i.e.

$$C = \frac{C_{POLY} + \beta^2 C_{OX}}{(1+\beta^2)} \tag{3}$$

where $\beta = R_{OX}/R_{POLY}$. Thus, if $C_{POLY} = 18$ nF/cm^2 and $C_{OX} = 600$ nF/cm^2, to yield a measured low-frequency capacitance of 110 nF/cm^2 then $\beta = 0.43$. Inserting this value into Eq. (1) requires that $R_{OX} = 890\ \Omega$ and $R_{POLY} = 2$ kΩ to give a relaxation frequency $f_R = 200$ kHz in Figs. 3a and 5. Ascribing these values to the DC resistance of the device yields a DC current density of 35 mA/cm^2 at 1 V, which is significantly higher than observed after capacitive switching. We may conclude, therefore, that the device does not behave homogenously over the entire electrode area.

The admittance data can be explained however when we assume a patchy conductance in the polymer film. The corresponding equivalent circuit for a film composed of two areas of different polymer conductivity is now given in Fig. 9. In this case, only that fraction of the device area with a low polymer resistance (Region 1) gives rise to the Maxwell–Wagner dispersion seen in Figs. 3a and 4, the rest of the device area (~83%) remaining in the high resistance state. Applying Eqs. (2) and (3) we now conclude that for the conductive region, $R_{POLY1} = 770\ \Omega$ which is close to the value required to fit the plots in Fig. 4 (see Table 1). This model requires that the condition $R_{OX1} \gg R_{POLY1}$ still applies in this region of the device so that the oxide layer limits the current through the device. Noting the values of R_{OX} in Table 1, the DC currents expected at 1 V are ~20 μA/cm^2 and 140 μA/cm^2 for the two switched

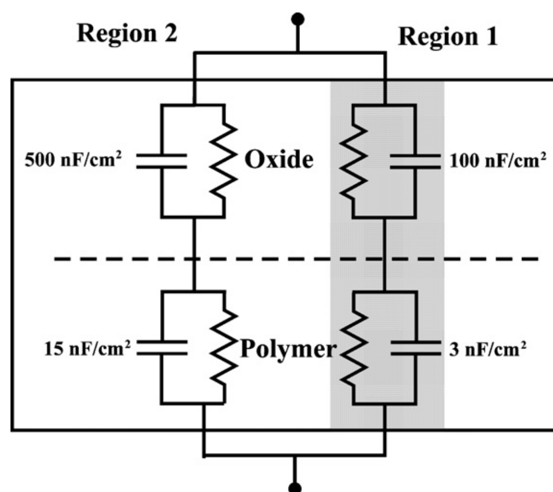

Fig. 9. Equivalent circuit for a film composed of two areas of different polymer conductivity. In this case, only that fraction of the device area with a low polymer resistance (Region 1) gives rise to the Maxwell–Wagner dispersion seen in Figs. 3a and 5, the rest of the device area, (~83%) remaining in the high resistance state (Region 2).

states and consistent, therefore, with the range of currents observed experimentally between the fully OFF and fully ON states (Fig. 2).

A further possibility is that the oxide layer is not uniform. To explain the capacitance data in Figs. 3a and 4 we must now assume that over ~83% of the device area (Region 2), the oxide capacitance is shunted by an oxide resistance that is much smaller than that of the corresponding area of polymer. Applying Eq. (2) to this fraction of the device and (i) replacing R_{POLY} with R_{OX2} and (ii) noting that the relaxation time of this part of the device must lie well below the measurement range, i.e. $f_R \ll 100$ Hz if the oxide in this region is not to contribute to the measured capacitance, then we may deduce that $R_{OX2} \gg 30$ MΩ. Since $R_{POLY2} \gg R_{OX2}$ the expected DC current densities at an applied voltage of 1 V from this part of the device will be much less than 3 μA/cm^2 and closer to that expected for the fully OFF state suggesting that the premise on which this model is founded is likely to be unsound.

Of the models proposed above, that based on a non-uniform polymer conductivity is the most plausible. However, the microscopic origin is as yet unknown.

Clearly, further work is necessary to clarify fully the nature of capacitive switching. Nevertheless, the general principles have been established. The device is described by a two layer model. The resistive switching reported by other workers is now seen

to be preceded by capacitive switching in which the conductance of one of the layers, probably that of the polymer, must increase substantially to explain the Maxwell–Wagner dispersion. The increased electric field now appearing across the oxide due to electron accumulation enhances minority carrier (hole) injection from the Al electrode, which is the likely cause of the dip in the *C–V* plots and the shoulder in the forward *I–V* characteristic observed in some devices after capacitive switching. Higher voltages lead to increased electrical stress across the oxide, further reducing the oxide resistance, which we surmise is the current limiting layer controlling the low-frequency loss in Figs. 3a and 4 following capacitive switching.

If, indeed, the conductance of the polymer is not homogeneous, the additional rise in capacitance and accompanying increase in loss in the fully ON state in Fig. 5 may simply reflect increased contributions from previously non-conducting regions of the device.

4. Conclusions

Summarizing, this admittance study shows that switching is a two-stage process. Initially, hole injection must be switched on at the aluminum electrode, we assume that this occurs as a result of electron trapping near the aluminum electrode. Hole injection will fill states in the aluminum oxide creating a dipole layer at the oxide/polymer interface. The high field across the oxide increases, thus encouraging injection of extrinsic charges into the polymer. The polymer resistance decreases substantially shunting the polymer capacitance and giving rise to a Maxwell–Wagner dispersion. We have termed this first step capacitive switching. Higher external applied voltages lead to increased electrical stress across the oxide reducing the oxide resistance and causing resistive switching.

The admittance data analysis also shows that the device does not behave homogenously over the entire electrode area, only a relatively small fraction of the device area (20%) gives rise to switching, the rest of device area remains in a high resistance state.

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