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Organic Materials for Active Layers in Transistors: Study of the Electrical Stability Properties

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Abstract. Field effect transistors based on several conjugated organic materials were fabricated and assesed in terms of electrical stability. The device characteristics were studied using steady state measurements as well as techniques for addressing trap states. Temperature-dependent measurements show clear evidence for an electrical instability occurring above 200 K that is caused by an electronic trapping process. It is suggested that the trapping sites are created by a change in the organic conjugated chain, a process similar to a phase transition.

Introduction

Conjugated organic materials can be used to build organic transistors for applications in integrated circuits or as pixel switches for displays. However, the reliability of organic based electronic circuits is limited by the electrical instability known as "gate-bias stress effect". This can be a severe limitation to the development of technological applications. Devices suffering from gate-bias stress effects exhibit threshold voltage shifts, ΔV_{th} and a slow and continuous decrease in the device current. Bias stress effects have been reported for a variety of organic based thin-film transistors (TFTs) [1-6]. In an attempt to understand the physical origin of this instability, several authors studied the effect using different dielectric materials [1,3], different types of silicon oxide as well as different surface treatments [6]. The data available in the literature suggest that stress in organic based devices is related to the properties of the organic semiconductor itself and is independent of the choice of gate dielectric. Supporting this view is the observation that stress can be removed when the device is illuminated with band-gap light [6,7]. Street *et al.* [7] suggest that the effect arises from the formation of trapped bound hole pairs (bipolarons). The formation of these bipolarons depletes the accumulation channel of mobile holes, thus causing an increase in the threshold voltage. Since the polaron binding energy can be dependent on the structural disorder and impurities (such as oxygen), this model explains how the device stability can be dependent on the sample preparation and handling.

Recently we showed [8] that gate-bias-stress effects have complex temperature dependence, dominated by two processes, one occurring near 220 K and the other close to room temperature. In this article a detailed study of this temperature-dependence is presented. Furthermore, different conjugated materials and polymer blends were compared with respect to their electrical stability. It is argued that the abrupt transition occurring near 200 K can be caused by a structural change in the molecule, such as a ring twist. Since some materials can be more prone to this changes than others, this can put new constrains in selecting conjugated materials for transistor applications.

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Results and discussion

The conjugated organic semiconductors used in this study are shown in Fig. 1. The α-sexithiophene (α-T6) and terrylene thin films were deposited by thermal sublimation in an ultra-high vacuum organic molecular beam deposition apparatus. Poly(3-hexythiophene) (P3HT) and [6,6]-phenly-C_{61}-Butyric acid methyl ester PCBM, were deposited by spin coating. Transistor test substrates were fabricated from a heavily n-doped silicon wafer with a thermally grown SiO_2 insulating layer and a patterned gold layer as the source and drain electrodes. Typical channel dimensions were W/L = 20,000 μm/10 μm. All the electrical measurements were carried out in vacuum (10^{-6} mBar).

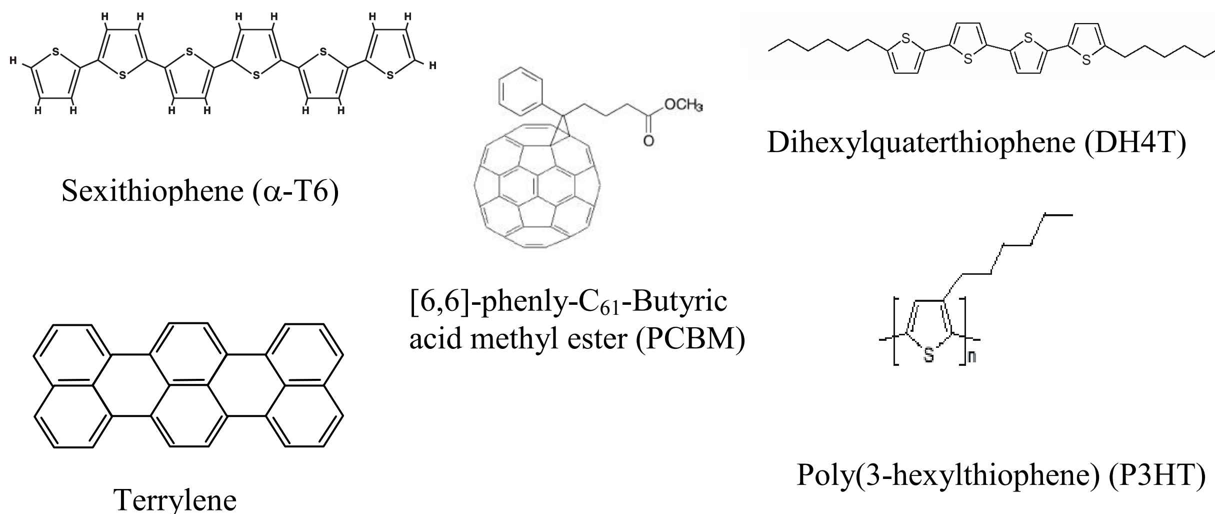

Fig.1.The molecular structure of the materials used in this work.

The transistors used in this study exhibit good characteristics with field effect mobilities in the order of 10^{-2} cm^2/Vs. The output characteristics (I_{DS}-V_{DS}) show current saturation as well as negligible contact resistance (see Fig. 2.)

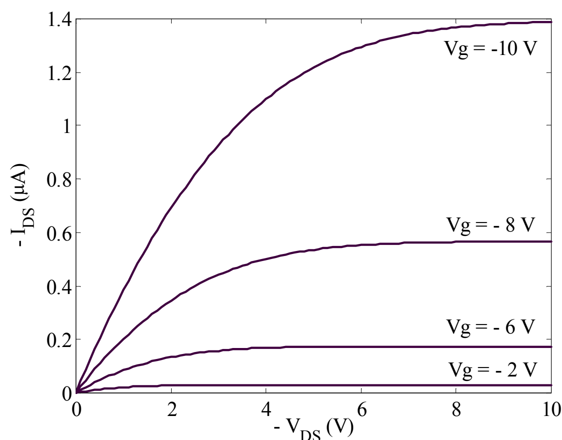

Fig. 2. Typical output characteristics of a sexithiophene thin film transistor.

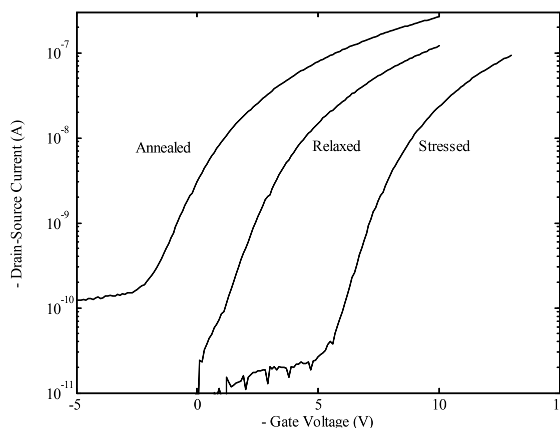

Fig. 3. Transfer curves for a sexithiophene device obtained for V_{DS} = – 0.5 V.

Fig. 3 shows three transfer curves of a typical device measured in the linear region (V_{DS} = –0.5 V). Theses curves correspond to three states, designated here as (a) annealed, (b) relaxed, and (c) stressed state. When devices are left resting for long periods of time (longer than one day), they exhibit a transfer characteristic named relaxed

state. This curve will suffer a parallel shift to higher threshold voltages without any variation of the subthreshold slope or the transconductance, if a negative gate bias is applied; we say the device becomes stressed.
Gently heating the device to 340 K with a positive gate bias applied will bring the threshold voltage to a positive value (bias-annealed state). The transfer curve will correspond to a device, which has a channel open for $V_g = 0$ V, and it is usually known as a “normally on” FET. The ΔV_{th} shift is large for negative biasing and small for bias-annealing.
The changes between the three states are entirely reversible. The bias-anneal state will relax to the relaxed state in a time scale of a few minutes. The kinetics of the stressed state have been previously reported by us to follow a stretched exponential behaviour [8], in agreement with a phenomenological description used in studies of stability in a-Si TFTs [9-11].
In order to shed some light onto the possible mechanism causing stress, the temperature dependence of the drain current was measured with a continuous negative gate voltage applied (stressing). A typical result is shown in Fig. 4.

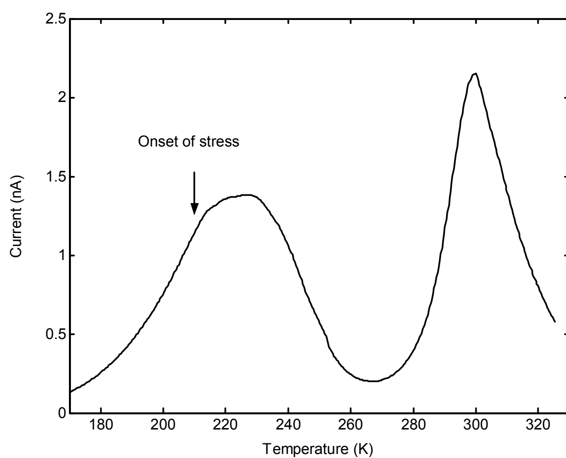

Fig. 4. Temperature dependence of the drain current showing the collapse in the current occurring at 220 K and near 300 K Measurements done in the linear region (V_{DS} = –0.5 V and V_g = –12 V) for a sexithiophene device.

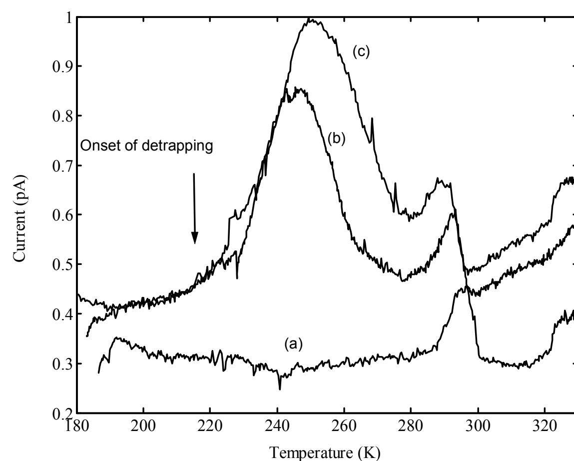

Fig. 5. Thermal detrapping curves measured at different heating rates and with different bias-filling conditions. (b) with a heating rate of 27.8 mK/s and (c) of 43.7 mK/s using a bias filling of –10 V. Curve (a) was recorded without bias-filling, although the device was bias-annealed according to the procedure described in the text.

In these experiments, the relaxed devices are first cooled down to 100 K without bias and then, while the drain current is being measured in the linear region (V_{DS} = – 0.5 V) for a constant bias V_g = –10 V, they are heated to 340 K with a constant heating rate.
For all gate voltages the drain current initially increases exponentially with the temperature, as expected. However, at approximately 220 K the current passes through a maximum before decreasing with further rise in temperature. This decrease in current is caused by a continuous increase in the device threshold voltage.

Therefore, we conclude that the stress-induced threshold voltage shift occurs only above 220 K. Below this temperature we observe that the threshold voltage is stable.

Above 280 K, the device current increases again before a second maximum sets in at around 310 K. In the temperature range [280–300 K] the current tends to recover. Above 300 K the current sharply decreases and stress effects dominate again. These results suggest there are two mechanisms involved.
Subsidiary experiments have shown that the low temperature stress process correlates well with a thermal detrapping current which can be recorded by freezing a stressed device to 100 K and then warming-up it to room temperature with a defined heating ramp, while the drain-source current is recorded in the absence of V_g.
Fig. 5 shows two typical detrapping currents with a peak near 250 K obtained for different heating rates. Also shown is a curve without stressing the device when cooling down; where the peak at 250 K disappears. This clearly shows that the detrapping current is related to the stress mechanism. Furthermore, comparing the curves in Fig. 4 and Fig. 5 it is clearly visible that the onset of the detrapping current coincides exactly with the temperature value (220 K) where stress becomes effective. This suggests that these both processes are interrelated. Since, below 220 K we cannot stress the device even using high electric fields, it means that the electronic states are not available below 220 K. Therefore they must be created by some mechanism. We suggest that the first stressing process (occurring at 220 K) is due to a trapping site created by some kind of structural change in the organic molecule. This structural modification can be for instance a twist in the thiophene ring. The sharp current collapse observed above room temperature is likely to be due to the contribution of a deeper state.
Stress effects were also studied in a number of other semiconductors such as DH4T, P3HT, terrylene, and a mixture of two materials P3HT/PCBM. Fig. 5 compares the temperature dependence of drain-source currents for transistors based on different semiconductors. It is interesting to note that the current collapse near 220 K is common to the majority of the materials studied, despite the fact that they were processed in different ways. P3HT was deposited by spin-coating while the DH4T and the sexithiophene were deposited by vacuum sublimation. Striking is also the observation that a mixture of P3HT/PCBM is almost stable against stress effects. Another material that we observed to be stable against electrical stress is terrelyne (see molecular structure in Fig. 1).

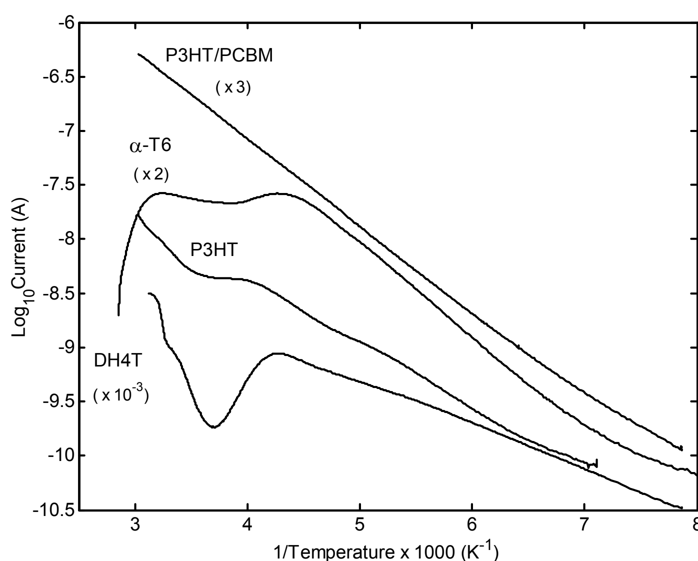

Fig. 6. Temperature dependence of the drain current measured in the linear region of different transistor devices based in different materials. The curves were shifted for clarity.

The above results support the view that gate-bias induced stress can have its origin in a structural relaxation of the semiconductor chain. The terrylene fused ring structure is more rigid and inhibits ring-rotation known to be an obstacle to π-conjugation and also inhibits Peirls distortion through bond length alternation by inclusion of all CC bonds in aromatic rings. Thus the susceptibility to local distortions upon charging can be reduced. A polymer blend such as the P3HT/PCBM is likely to have a similar effect by reducing the degrees of freedom of the polymer chain.

Conclusions

In conclusion, thermal detrapping currents provide strong evidence that the gate-bias induced stress in organic based transistors, is due to trapping of charge carriers in the organic semiconductor. It is suggested that these traps have origin in a structural relaxation of the organic chain, occurring near 220 K for thiophene based materials. The temperature at which the relaxation occurs is apparently independent of the thin film processing conditions. Conjugated materials which do not allow easily for a ring-rotation, or that are constrained in blends, are quite stable against electrical stress. This may put new restrictions in the selection and design of organic semiconductors for transistor applications.

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References

[1] A.R. Brown, C.P. Jarret, D.M. de Leeuw, and M.Matters: Synth. Met. Vol. 88 (1997), p. 37
[2] M. Matters, D.M. de Leeuw, P.T. Herwig, and A.R. Brown: Synth. Met. Vol. 102 (1999), p. 998
[3] S.J. Zilker, C. Detchverry, E. Cantatore, and D.M. de Leeuw: Appl. Phys. Lett. Vol.79 (2001), p. 1124
[4] W.A. Schoonveld, J.B. Oosting, J. Vrijmoeth and T.M. Klapwijk: Synth. Met. Vol. 101 (1999), p. 608
[5] J. Yuan, J. Zhang, J. Wang, D. Yan and W. Xu: Thin Solid Films, Vol. 450 (2004), p. 316
[6] A. Salleo and R.A. Street: J. Appl. Phys: Vol. 94 (2003), p. 471.
[7] R.A. Street, A. Salleo, M. Chabinyc: Phys. Rev. B, Vol. 68 (2003), p. 085316.
[8] H.L. Gomes, P. Stallinga, F. Dinelli, M. Murgia, F. Biscarini, D.M. de Leeuw, T. Muck, J. Geurts, L.W. Molenkamp and V.Wagner: Appl. Phys. Lett. Vol. 84 (2004), p. 3184
[9] B. Stannowski, R.E.I Schropp, R.B. Wehrspohn and M.J. Powell: J. of Non-Cryst. Solids Vol. 299 (2002), p. 1340
[10] S.C. Deane, R.B. Wehrspohn, and M.J. Powell: Phys. Rev. B. Vol. 58 (1988), p. 12625
[11] R.B. Wehrspohn, S.C. Deane, I.D. French, I.G. Gale, M.J. Powell and R. Brüggemann: Appl. Phys. Lett. Vol. 74 (1999), p. 3374