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Section 21. Devices. I. Inorganic and organic thin film transistors. c. Organic based

The effect of water related traps on the reliability of organic based transistors

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Abstract

The electrical stability of metal–insulator–semiconductor (MIS) capacitors and field-effect transistor structures based in organic semiconductors were investigated. The device characteristics were studied using steady state measurements AC admittance measurements as well as techniques for addressing trap states. Temperature-dependent measurements show clear evidence that an electrical instability occurs above 200 K and is caused by an electronic trapping process. Experimental results show that water is responsible for the trapping mechanism.
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1. Introduction

There is considerable interest in instability mechanisms in organic field-effect transistors. The most important instability is the threshold voltage shift that is observed after prolonged application of a gate voltage also known as bias-stress. This effect shows as a continuous decrease in the device current when the gate bias is kept constant. As a consequence, to maintain a constant current level, the gate voltage must be continuously increased, in other words the threshold voltage is constantly increasing.

This instability has been studied extensively because of its practical importance in the envisaged device applications, such as flexible displays and wireless identification transponders. Stress effects are commonly reported in the literature for a variety of transistors prepared using different techniques, different dielectric layers, as well as different organic semiconductors [1–7]. The effect has been explained as due to a slow trapping of charge carrier in defects of unknown origin [3]. It is known that the current degradation is faster when the devices are exposed to water vapor atmosphere [4], moreover it has also been reported that the device electrical stability improves after heating the devices in high vacuum [8].

Despite these evidences, a clear correlation between water contamination and stress has never been established. The reason lies in the observation that stress is absent below 200 K and starts only above that temperature. Furthermore, there are no pronounced effects near the well-known critical temperature of 273 K.

In order to establish a relation between water and stress, we compare the electrical behavior of a sample in its as-grown state, with its electrical characteristics after being deliberately exposed to water vapor. As a sensitive probe, we use the temperature dependence of the device current for a particular stable sample.

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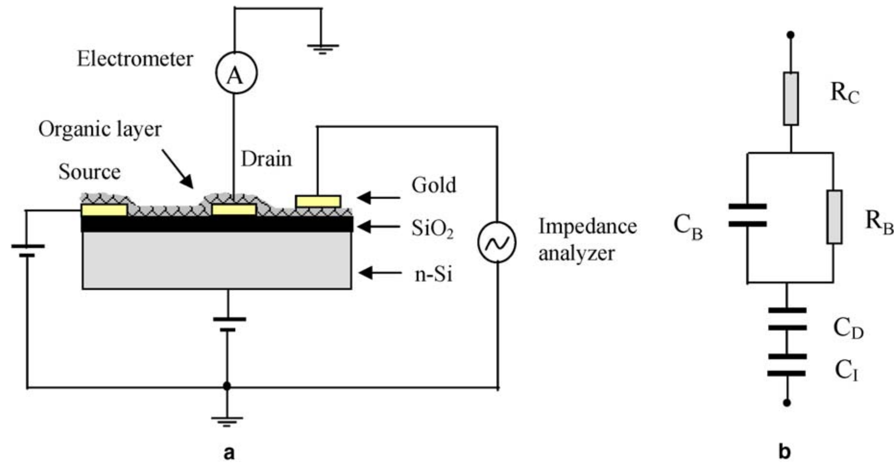

Fig. 1. (a) Schematic diagram of the device structure used and (b) equivalent circuit representing an ideal polymer MIS capacitor.

2. Experimental details

Transistor test substrates were heavily n-doped silicon wafers with a thermally grown SiO_2 insulating layer (200 nm) and patterned gold as the source and drain electrodes. These electrodes provide a channel length of 10 μm and a channel width of 10000 μm. The substrates were passivated by hexamethyldisilazane (HMDS), before deposition of the active layer. Metal–insulator–semiconductor capacitors were fabricated by evaporating a gold electrode on top of the organic layer. Fig. 1 shows the device schematics.

Poly(3-hexythiophne) (P3HT) and polyarylamine (PAA) thin films were deposited by spin-coating. The polyarylamine device was subsequently annealed in N_2 environment for 1 h at 100 °C. Film thickness varies between 20 nm for poly(3-hexylthiophene) thin films to 57 nm for the polarlylamine film.

Electrical measurements were carried out using a Keithley 487 picoammeter/voltage source and an Oxford temperature controller ITC 601. AC admittance measurements were made using a Fluke PM 6306 LCR meter over the frequency range 50 Hz–1 MHz. The signal amplitude was 400 mV.

Wet-atmosphere exposure was carried out by bubbling dry N_2 through distilled water poured into a sealed flask. After this, the sample chamber was pumped to high vacuum for 20 min prior to any electrical measurements.

The devices do not show contact problems, they have a threshold voltage in the range of 2–4 V and the mobilities are of the order 10^{-3} $cm^2\ V^{-1}\ s^{-1}$.

3. Results

Fig. 2 shows the temperature dependence of the drain–source current measured in the linear region for two different devices. The drain current initially increases exponentially with temperature, as expected. However, just at around 200 K a change in slope is noticeable for all the devices. In polyarylamine device the change is abrupt at 200 K causing a pronounced deep. For poly(3-hexylthiophene) the change is only visible as a decrease in slope starting to occur at 200 K. These changes at 200 K observed in the Arrhenius plots are due to a decrease in the drain–source current for a constant gate bias. The current decrease is caused by strong trapping, which depletes the sample from free charge carriers and is the origin of stress effect. Below 200 K the device is stable, as also previously reported [9]. It is worthwhile to mention that the position in temperature (200 K) of the anomaly for a particular sample is independent of the heating rate and gate bias applied.

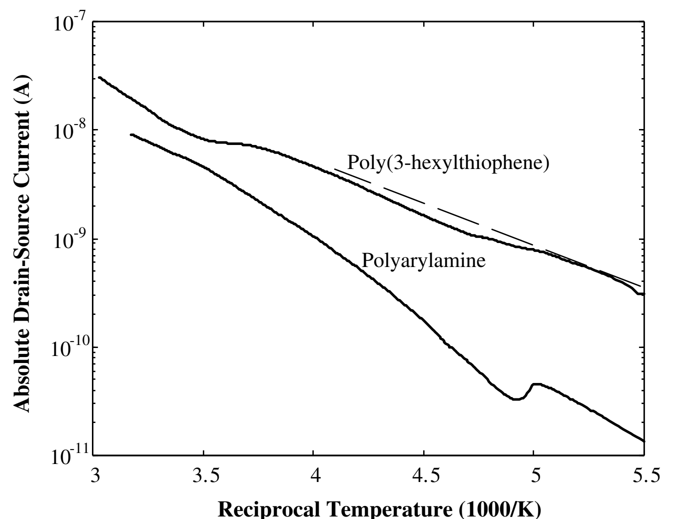

Fig. 2. Temperature dependence of the drain current for two transistor devices fabricated using different active layers. The curves were measured in the linear region (typical bias voltages: $V_G = -10$ V and $V_{DS} = -0.5$ V). The heating rate was 2 K/min for all the curves. The dashed line is a guideline for the eye.

Near room temperature further changes are observed in the device current caused again by carrier trapping. It is remarkable that the changes are occurring coincidently at 200 K, for different materials. Furthermore, a similar tran-

sition temperature was also reported for poly(3,3‴-dialkyl-quarterthiophene) by Salleo and Street [10], who observe that the device current exhibits its fastest decay at 220 K.

Although, all the devices show a common anomaly at 200 K, Fig. 2 also shows some differences in the magnitude of the process. While in the sexithiophene device trapping is quite pronounced, in the poly(3-hexylthiophene) the effect is relatively week. The differences may be related to different processing and handling conditions (of materials and substrates) as well as due to different morphologies.

The anomalies occurring in the transistor DC current can also be observed in AC admittance measurements in metal–insulator–semiconductor (MIS) capacitors. For poly(3-hexylthiophene) devices the AC loss (conductance/($2\pi f$)) exhibits two major relaxation peaks, a high frequency one (near 1 MHz) which we believe is due to the device geometrical structure according to the equivalent circuit in Fig. 1(b), and a low frequency relaxation process occurring near 2 kHz, see Fig. 3. This low frequency process shows a peculiar temperature dependence. This can be seen by plotting the associated capacitance measured at 1 kHz as a function of temperature as shown in Fig. 4. It is clearly visible that an extra capacitance comes in at approximately 200 K and reaches it maximum value at temperatures near 270–280 K. Above that, the extra capacitance decreases rapidly and at 300 K device capacitance follows again the normal behavior. This behavior correlates quite well with the changes observed in the transistor DC current (see Fig. 2 for the poly(3-hexylthiophene device)). It is quite interesting that the extra capacitance starts to disappear at a temperature very close to the water critical point 273 K.

The fact that the 200 K anomaly is relatively independent of the materials suggest that is related with an extrinsic and very common impurity, which we will show is water.

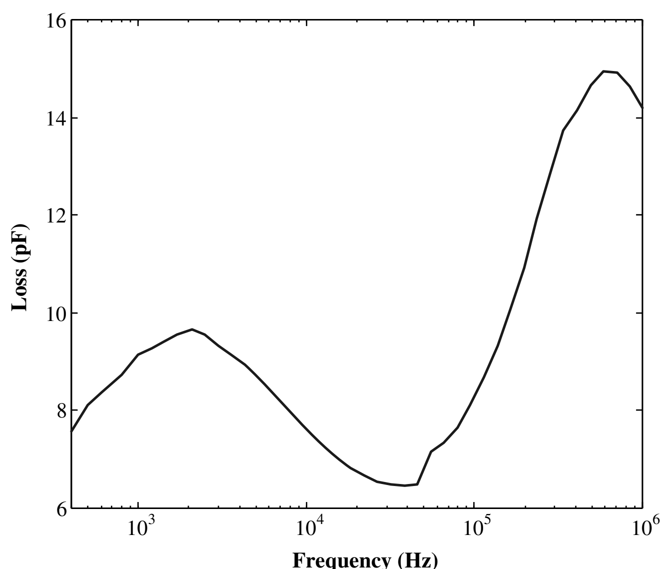

Fig. 3. Frequency-dependence of the measured loss (conductance/($2\pi f$)) of the MIS capacitor. The Maxwell–Wagner dispersion due to the device structure is clearly visible near 1 MHz. The low frequency relaxation is likely to be due to trap states.

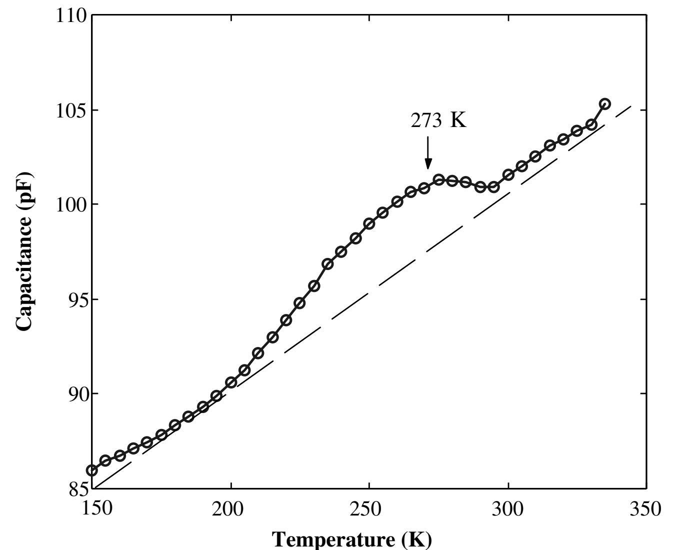

Fig. 4. Temperature dependence of the MIS capacitance measured at the frequency of 1 kHz.

To prove that water is responsible for the process occurring at 200 K a particular stable sample of polyarylamine (without anomalous behavior) was selected and deliberated exposed to water vapor. It is important to note that in the as-grown stage, the polyarylamine device was annealed in N_2 environment for 1 h at 100 °C.

Fig. 5 shows the experimental data represented in an Arrhenius plot. The sample in its as-grown stage exhibits almost a perfect straight line. The absence of anomalies in the temperature dependence of the current reflects a high electrical stability. After deliberately being exposed to water vapor for 24 h and pumped again in high vacuum

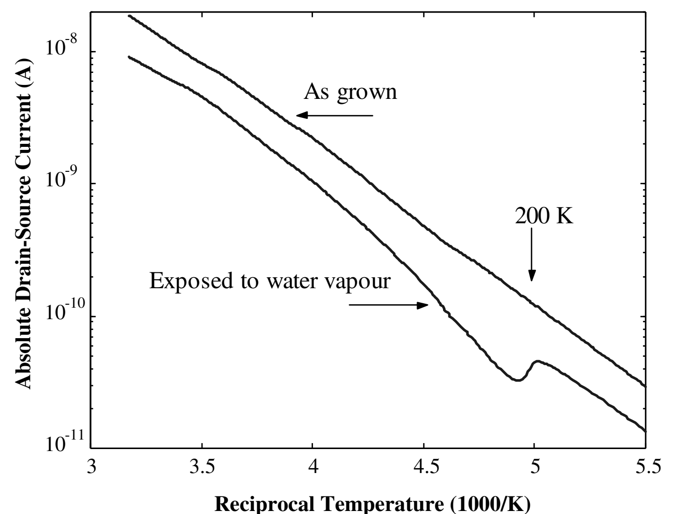

Fig. 5. The effect of water exposure in the temperature dependence of the drain–source current measured in the linear region ($V_{DS} = -1$ V and $V_G = -8$ V) and plotted in Arrhenius form.

prior to the electrical measurements, an anomalous current decrease appears suddenly at around 200 K.

4. Discussion

Water molecules, when confined, are unable to form a crystalline structure; thus water remains fluid, well below 273 K. It is then called super-cooled water or glassy water. There is a rich and extensive literature about the behavior of super-cooled water, for instance see the review [11]. In the context of the present work, the most relevant is that this metastable form of water has a phase transition at around 200–220 K [12–17]. In between 200 and 273 K the water is a metastable mixture of the two liquid phases. Apparently, water above 200 K can already trap charge carriers in a very effective way. Furthermore, this means that at the critical temperature of 273 K we do not have a conventional solid–liquid phase transition, but something like a change from a metastable liquid form to a liquid form of water and the trapping efficiency is not much altered by this transition. This may explain that at 273 K the changes are not as significant as expected even after water exposure.

5. Conclusions

In summary, we demonstrated that charge carrier trapping starts to occur at 200 K and causes a threshold voltage shift in transistor devices. These trap states are relatively shallow, therefore, as the temperature rises the carrier trapping becomes less effective and the device can recover. However, above 280 K a second and deeper trapping process sets in, causing a pronounced and long-lived threshold voltage shift.

The temperatures at which the trapping process occurs, correlates very well with the phase transitions known to occur in confined water. Therefore, we conclude that trapped water is likely to be the main source for the electrical instability observed above 200 K. We believe that shallow trapping below 273 K is due to the presence of a metastable form of liquid water. Above 280 K liquid form of water can act as a deep trap state. This finding is in agreement with observations that stress effects are suppressed or substantial reduced after annealing [8].

We are convinced that research should be oriented to prevent the incorporation of water, either by introducing hydrophobic capping layers or by molecular design of new materials less susceptible to water incorporation.

Acknowledgments

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