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Bias-induced threshold voltages shifts in thin-film organic transistors

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An investigation into the stability of metal-insulator-semiconductor (MIS) transistors based on α-sexithiophene is reported. In particular, the kinetics of the threshold voltage shift upon application of a gate bias has been determined. The kinetics follow stretched-hyperbola-type behavior, in agreement with the formalism developed to explain metastability in amorphous-silicon thin-film transistors. Using this model, quantification of device stability is possible. Temperature-dependent measurements show that there are two processes involved in the threshold voltage shift, one occurring at $T \approx 220$ K and the other at $T \approx 300$ K. The latter process is found to be sample dependent. This suggests a relation between device stability and processing parameters. © *2004 American Institute of Physics.* [DOI: 10.1063/1.1713035]

One of the most important stability issues in organic transistors is the shift in the threshold voltage upon applying a bias to the gate electrode, so-called stressing. The applied negative gate potential for a p-type semiconductor causes a buildup of mobile charges at the semiconductor/insulator interface, which are then trapped. As a consequence, to reach an identical channel current subsequently, a higher gate voltage has then to be used. Bias stress effects have been reported for transistors based on pentacene, polythienylene vinylene[1–3] α-sexithiophene[5] poly-9,9-dioctyl-fluorene-co-bithiophene and regioregular-polythiophene.[5,6] In an attempt to understand the physical origin of this instability and the exact location of the trapped charges, several authors have studied the effect using different dielectric materials,[1,3] different types of SiO_2, and different surface dielectric treatments.[5] It is well established that ionic movements in thermally grown SiO_2 do not occur. Therefore, the data available in the literature suggest that stress in devices using thermally grown SiO_2 is related to the properties of the organic semiconductor itself. Recent work has also shown that the bias stress effect can be reversed by band gap light,[5] confirming the view that the stress effect is due to trapped charges located within the semiconductor film, near the dielectric interface. Several authors have also reported that the threshold voltage shift is reversible, and that the recovery process can be enhanced by a positive gate bias.[1,4]

Although important progress has been made in determining the location of the trapped charges induced by voltage stressing, a limited number of systematic studies have been reported concerning the dependence of the bias stress effects on the processing parameters and materials.[6] It is known that some devices are more prone to this instability than others, even when they are made from the same organic materials and fabricated under similar conditions. The key to these differences should reside in the processing and handling conditions. Therefore, to establish a correlation between processing parameters and electrical stability it is important to be able to quantify the electrical stability. In this letter we show that formalism developed for amorphous silicon thin film transistors (a-Si TFTs) can be also applied to α-sexithiophene (α-T6) thin-film transistors and used to quantify the device stability.

The α-T6 thin films were deposited by thermal sublimation in a ultrahigh vacuum organic molecular beam deposition apparatus (base pressure 10^{-9} mBar) onto preformed TFT test substrates, consisting of a heavily n-doped silicon gate electrode, a 200-nm-thick (thermally grown) SiO_2 insulating layer ($C_{ox} = 19\ \mathrm{nF\,cm^{-2}}$), and a patterned gold layer as the source and drain electrodes. The channel dimensions were $W/L = 20\,000/10\ \mu\mathrm{m}^2$. During the deposition, the sample substrate was held at 150 °C. Gate bias stress has been carried out in the linear regime using a voltage between drain and source terminals (V_{DS}) of -0.5 V. The transfer characteristics were rapidly measured following a predetermined stressing time. All the measurements were carried out in vacuum (10^{-6} mbar). The transistors used in this study exhibit good characteristics, with a low off current, and a field-effect mobility of $1.7 \times 10^{-2}\ \mathrm{cm^2/V\,s}$. The $I_{DS}-V_{DS}$ curves exhibit current saturation as well as negligible contact resistance (see Fig. 1).

Since in organic materials the transfer characteristics are often not linear, it is usually difficult to obtain a unique slope

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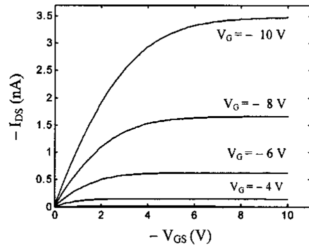

FIG. 1. Drain current against drain voltage characteristics measured for a range of gate voltages applied to a sexithiophene transistor.

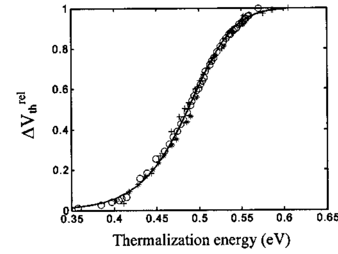

FIG. 3. Measured values of relative threshold-voltage shift at 290 K (*), 296 K (O), and 320 K (+) plotted as a function of thermalization energy (see text for details). The solid line represents the best fit based on Eq. (3).

and an intercept from which the mobility and the threshold voltage can be extracted. This problem is well known, and has been addressed in a-Si TFT technology,[7] as well as in organic based devices.[8–10] Usually it is considered that the parametric field effect mobility (μ_{FET}) increases with the gate voltage as $\mu_{FET} = \mu_0 (V_{GS} - V_{th})^{\gamma}$, where V_{th} is the threshold voltage, V_{GS} the gate-source voltage, and μ_0 and γ are empirical parameters defining the variation of the mobility with V_{GS}.

The drain current in the linear region, i.e., for small drain voltage and for $V_{GS} > V_{th}$ is then given by

$$I_{DS} = K(V_{GS} - V_T)^{1+\gamma} V_{DS}. \quad (1)$$

In the data analysis carried out herein, the linear transfer curves were plotted as $I_{DS}^{1/(1+\gamma)}$ versus V_{GS}. γ and V_{th} can be extracted from the experimental curve using an integral procedure proposed by Cerdeira *et al.*[7] Figure 2 shows the evolution of typical experimental transfer characteristics after negative gate bias stress, V_G of -10 V for different stress times and for $\gamma = 0.81$. As can be seen, the transfer curves are linear over an extended voltage range and it is possible to extract an unambiguous value for V_{th}. Moreover, the threshold voltage shift approaches the stressing gate voltage for long stressing times.

As previously reported by others[1,4] we also observe that V_{th} will recover to its original value if the device is left unbiased. The recovery can be enhanced if a positive gate bias is applied. Furthermore, if the device is slightly heated up with a positive gate bias it can be brought to a state where it even exhibits higher current levels and behaves as a normally ON device.

Previously, studies have reported that the time dependence of V_{th} upon stress follows a logarithmic law.[4] In our case we found that the time dependence of V_{th} is in agreementwith phenomenological description developed in studies of electrical stability in a-Si TFTs. For a-Si TFTs two major models were developed to explain V_{th} shifts.[11,12] Although

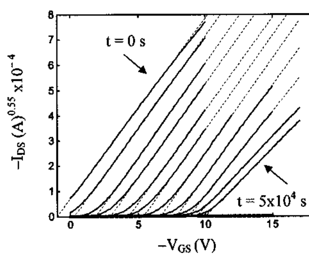

FIG. 2. Evolution of the linear transfer curves with increasing stress time, up to 5×10^4 s with $V_G = -10$ V. The curves are plotted following Eq. (1) in which $\gamma = 0.81$.

the underlying microscopic processes are different, in both models the creation of states is governed by a dispersive process, typical of amorphous materials. These models lead to a differential equation for the density of states created, ΔN_D, which is proportional to ΔV_{th}, since $\Delta N_D = C_{OX} \Delta V_{th}$. These states are the ones that must be filled before significant conduction can occur via accumulation layer. Based on these models it is readily shown that the rate of change in V_{th} is given by[13,14]

$$\frac{dV_{th}}{dt} \propto \frac{d(\Delta N_D)}{dt} \propto N_{BT}(t)^{\alpha} \frac{t^{\beta-1}}{t_0^{\beta}}, \quad (2)$$

Where the time constant t_0 is thermally activated, i.e., $t_0 = \nu^{-1} \exp(E_A/k_B T)$. Here E_A is the mean activation energy for trap creation. β is a dispersion parameter given by T/T_0, where $k_B T_0$ is the slope of the distribution in the activation energies for trap creation and ν an attempt to escape frequency. When $\alpha = 1$, Eq. (2) results in a stretched-exponential function $V_{th} \approx 1 - \exp[-(t/t_0)^{\beta}]$ commonly observed in disordered materials.[12,15,16] The parameter $N_{BT}(t)$ represents the concentration of carriers in the band tail states.

When applied to experimental threshold voltages shifts on a-Si TFT's, the stretched exponential gives a poor agreement. It was found that a better agreement was obtained for a-Si TFTs with α in the range of 1.5–1.9.[17] Furthermore several authors combined the stress time t and temperature T in a so-called thermalization energy $E_{th} = k_B T \ln(\nu t)$ which can be interpreted as all possible trap sites with $E_A \leqslant E_{th}$ have been filled at time t. Equation (2) then results in a stretched hyperbola:[13,18,19]

$$\frac{V_{th} - V_{th}^{ini}}{V_g - V_{th}^{ini}} = 1 - \frac{1}{\left[\exp\left\{\frac{E_{th} - E_A}{k_B T_0}\right\} + 1\right]^{1/(\alpha-1)}} \quad (3)$$

where V_{th}^{ini} is the initial threshold voltage and V_g the gate stress voltage.

Figure 3 shows the relative threshold voltage shift $\Delta V_{th}^{rel} = (V_{th} - V_{th}^{ini})/(V_g - V_{th}^{ini})$ in (α-T6) TFT's as a function of the thermalization energy for two bias stress experiments carried out at the temperatures of 296, 290, and 320 K. The experimental curves will fall in top of each other by selecting an appropriate attempt to escape frequency ν, which we find to be about 10^5 Hz. Reasonably good fits can also be obtained with slightly different values for the attempt to escape frequency; therefore the uncertainty of this fitting parameter is rather large. It is not possible to improve the accuracy of this parameter because the temperature range available to carry out the stressing experiments is quite narrow. As will

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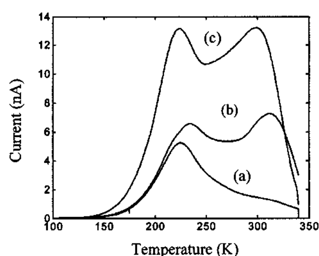

FIG. 4. Temperature dependence of the drain current, when the device is subjected to different gate voltages: (a) for $V_G = -7$ V, (b) for $V_G = -8$ V, and (c) for $V_G = -9$ V.

be discussed later, electrical stress dominates only in two narrow temperature ranges, one located in the range 220–250 K and one above 300 K. Temperatures above 320 K were not used to prevent other effects, such as thermal undoping. For fitting the present results (Fig. 3) we used the stretched-hyperbola formalism of Eq. (3), we used $\alpha = 1.5$ and $\nu = 10^5$ Hz. The only fitting parameters were E_A and $k_B T_0$, which were systematically changed to yield the best fit to the data. From the fitting we obtain $E_A = 0.52$ eV and $k_B T_0 = 33$ meV. Higher values for E_A reflect a higher stability; therefore, using this phenomenological approach it is possible to quantify the device stability.

In order to shed some light onto the possible mechanism causing the stress, we also measured the temperature dependence of the transfer curves and the drain current. The results are well exemplified by plotting the drain current as function of temperature for different gate voltages as shown in Fig. 4. In these experiments the devices are first cooled down to 100 K and then while the drain current is being measured they are heated to 340 K with a heating rate of 2.4 K/min. Below 220 K, the device threshold voltage is independent of time and only changes with temperature. Before a heating ramp is started the device usually remains for 10 min at 100 K. Experiments were also carried out where the device was held for periods as long as 1 h at 100 K and no changes in the threshold voltage were observed.

For all gate voltages the drain current initially increases with the temperature, as expected. However, at approximately 220 K the current passes through a maximum before decreasing with further increase in temperature. This anomalous decrease in the current is caused by a continuous increase in the device threshold voltage. Therefore, we conclude that the stress-induced instability in threshold voltage occurs only above 220 K. Below this temperature we observe that the threshold voltage is stable and insensitive to gate-voltage stressing. For gate voltages stronger than -7 V and temperatures above 290 K the device current rises again before a second maximum sets in at $T \approx 300$ K causing a decrease in the device current which is again due to a threshold voltage shift. While the first process is observed in all the samples studied and is always located at around 220 K, the second process is not always observed and the temperature at which it occurs varies significantly from sample to sample, suggesting that it is related to device processing parameters or sample handling. Similar results were recently reported for a solution-processed oligothiophene.[20]

Below 220 K the device current is thermally activated with activation energy of 0.2 eV, which is due to a thermal activation of the effective charge carrier mobility. Above 220 K the stress mechanism competes with the rise in mobility, therefore, the overall decrease in current is a convolution of the two processes. Furthermore, subsidiary stress experiments carried out in the first stressing region ($T = 240$ K) show that the activation energy for defect creation ($E_A \approx 0.3$ eV) is lower than the one observed at room temperature, suggesting that the mechanism responsible for stress is different at 240 K. This makes the analysis of both mechanisms in an independent manner very difficult.

In conclusion, we have shown that a phenomenological description used in studies of stability in a-Si TFTs is applicable to organic based transistors. Using this description physical meaningful parameters are extracted that can be used as an indication of the devices stability. In the framework of the exponential barrier model, the parameter E_A corresponds to the most probable energy barrier for defect creation or trap filling. We believe that some fabrication step is the key to understanding the instability. Further studies of the microscopic mechanisms of defect creation must to be undertaken to understand the effect and to ascertain whether it can be related to a measurable bulk property.

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