Electrical characterisation of transistors

Centre of Electronics Optoelectronics and Telecommunications, Faro, Portugal

Development of Novel Conjugated MOlecular NAnostructures by LIthography and their Transport Scaling Aspects (MONA-LISA).

OPTO-ELECTRONICS

UNIVERSIDADE DO ALGARVE

Wuppertal, January, 2003

Summary

- Data analysis (procedure for the extraction o TFT parameters).
- Transport mechanism in thin films of T6.
- New insights into the problem of meta-stability.
- Nano-FETs.
- Conclusions.

Procedure for the extraction of TFT parameters

LIN: $$I_{ds} = (W/L)\, C_{ox}\, \mu\, (V_g - V_t)^{1+\gamma}\, V_{ds}$$

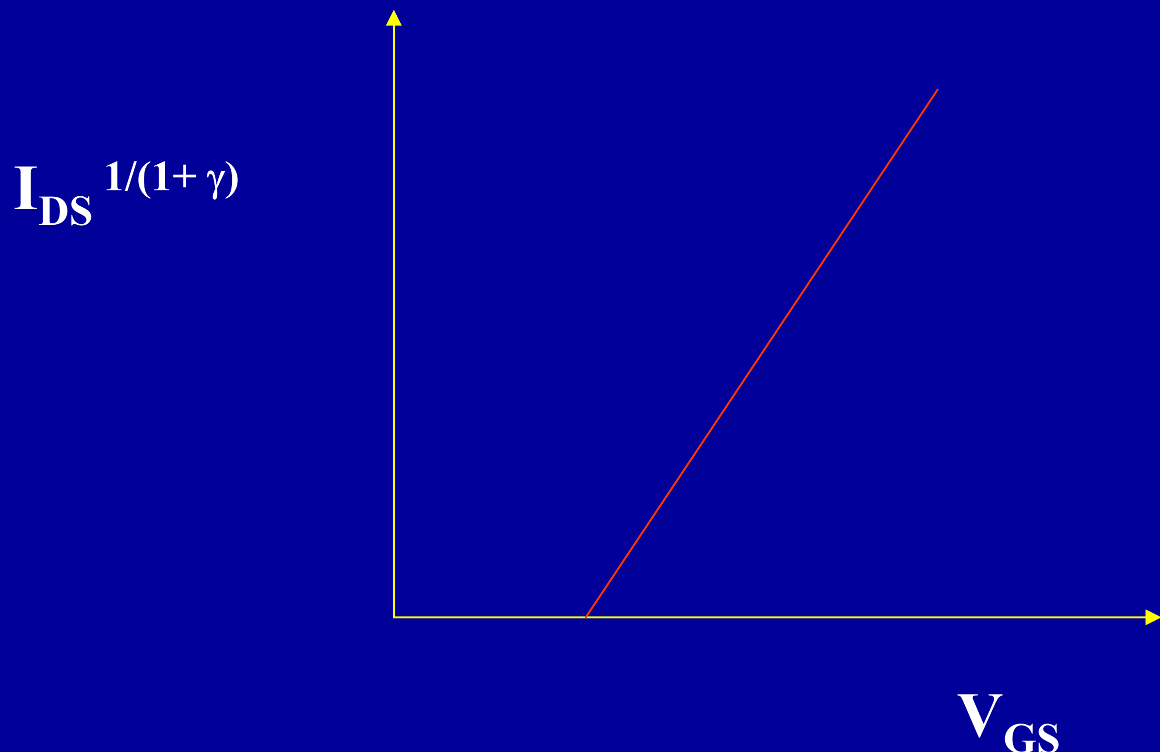
SAT: $$I_{ds} = (^1/_2)(W/L)\, C_{ox}\, \mu\, (V_g - V_t)^{2+\gamma}$$

This implies that the amount of free charge in the channel grows faster-than-linear with the gate voltage, i.e. no longer a simple "parallel metal plates" device

Alternatively: define an as-measured (parametric) mobility that depends on V_g, example (LIN)

$$I_{ds} = (W/L)\, C_{ox}\, \mu(V_g)\, (V_g - V_t)\, V_{ds}$$

Extraction procedure



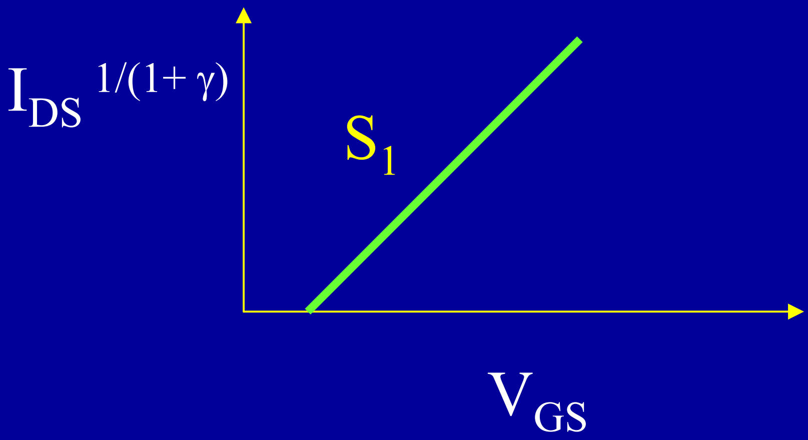
Extraction procedure

$$H(V_{GS}) = \frac{\int_0^{V_{GS}} I_{DS}(x)dx}{I_{DS}(V_{GS})} \quad \textbf{(1)}$$

$$H(V_{GS}) = \frac{1}{2+\gamma}\left(V_{GS} - V_T\right) \quad \textbf{(2)}$$

V_T is determined from the intercept, and γ from the slope

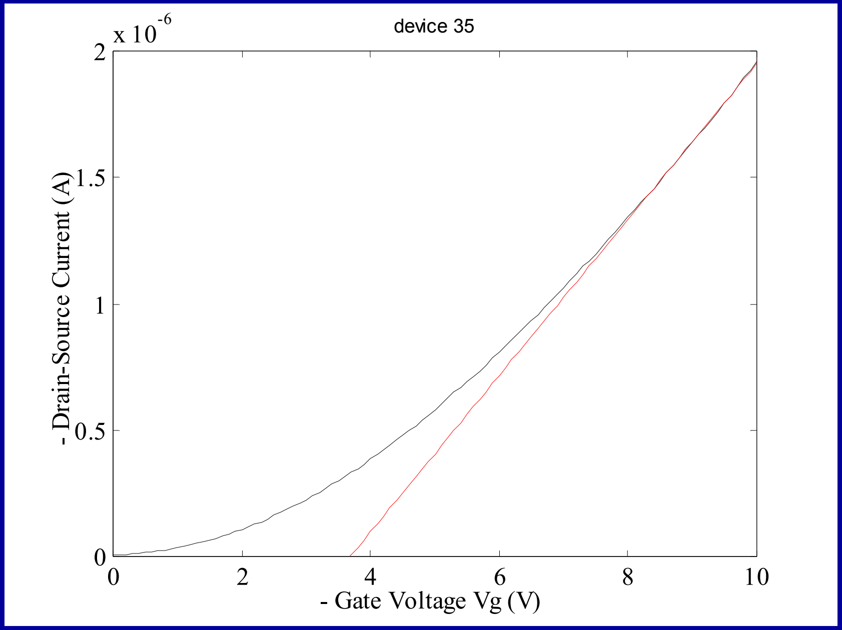
$$\textbf{(3)} \quad I_{DSlin} = \frac{K}{V_{AA}^{\gamma}}(V_{GS} - V_T)^{1+\gamma} V_{DS}$$

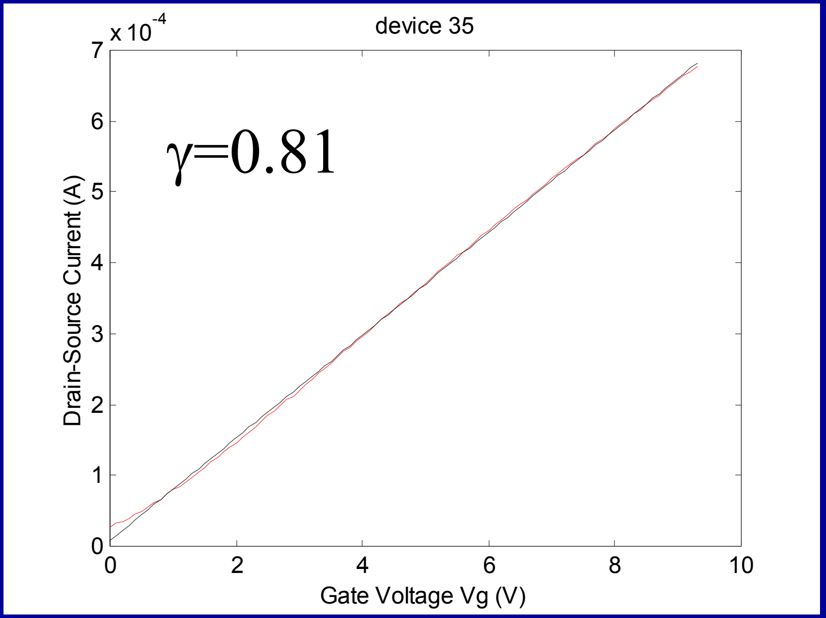


$$\textbf{(4)} \quad V_{AA} = \left[\frac{KV_{DS}}{S_1^{1+\gamma}}\right]^{1/\gamma}$$

$$\textbf{(5)} \quad \mu_{FET} = \mu_0\left(\frac{V_{GS} - V_T}{V_{AA}}\right)^{\gamma}$$

Exemple





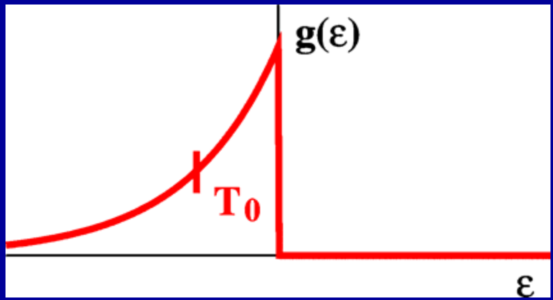
$$I_{DSlin} = K\mu(V_{GS} - V_T)V_{DS}$$

$$I_{DSlin} = \frac{K}{V_{AA}^{\gamma}}(V_{GS} - V_T)^{1+\gamma} V_{DS}$$

Variable Range Hopping

VRH involves decaying density of trap states, for example

$$\boldsymbol{g(\varepsilon) = (N_T/kT_0)\ \mathrm{exp}\ (\varepsilon/kT_0)}$$



Which results in, when the as-measured mobility in the linear region is defined as

$$\mu_{\mathbf{FE}}\ \mathrm{(def)}= \boldsymbol{(L/C_{ox}WV_{ds})\ \mathrm{d}I_{ds}/\mathrm{d}V_g}$$

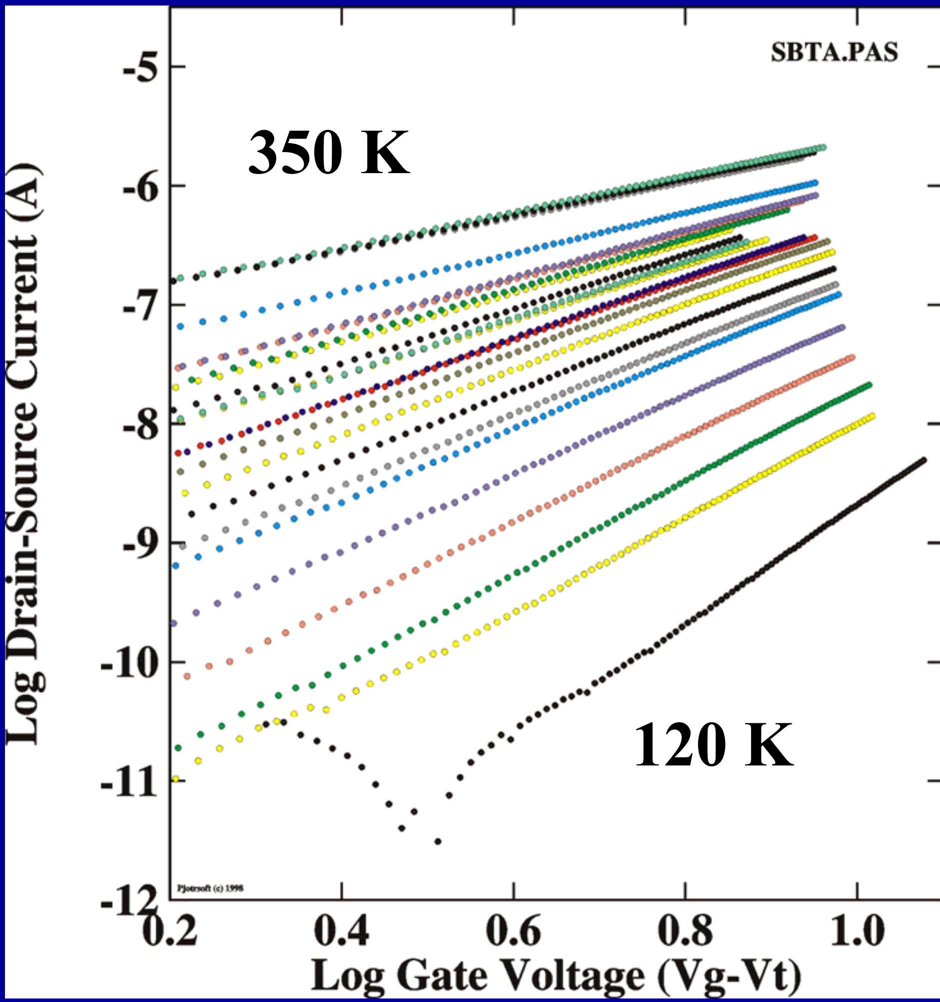
this mobility is

$$\mu_{\mathbf{FE}} = \mu_0(T)\ V_g^{\,2(T0/T-1)}$$

therefore

$$\boldsymbol{\gamma = 2(T_0/T-1)}$$

Obtaining γ as a function of *T*

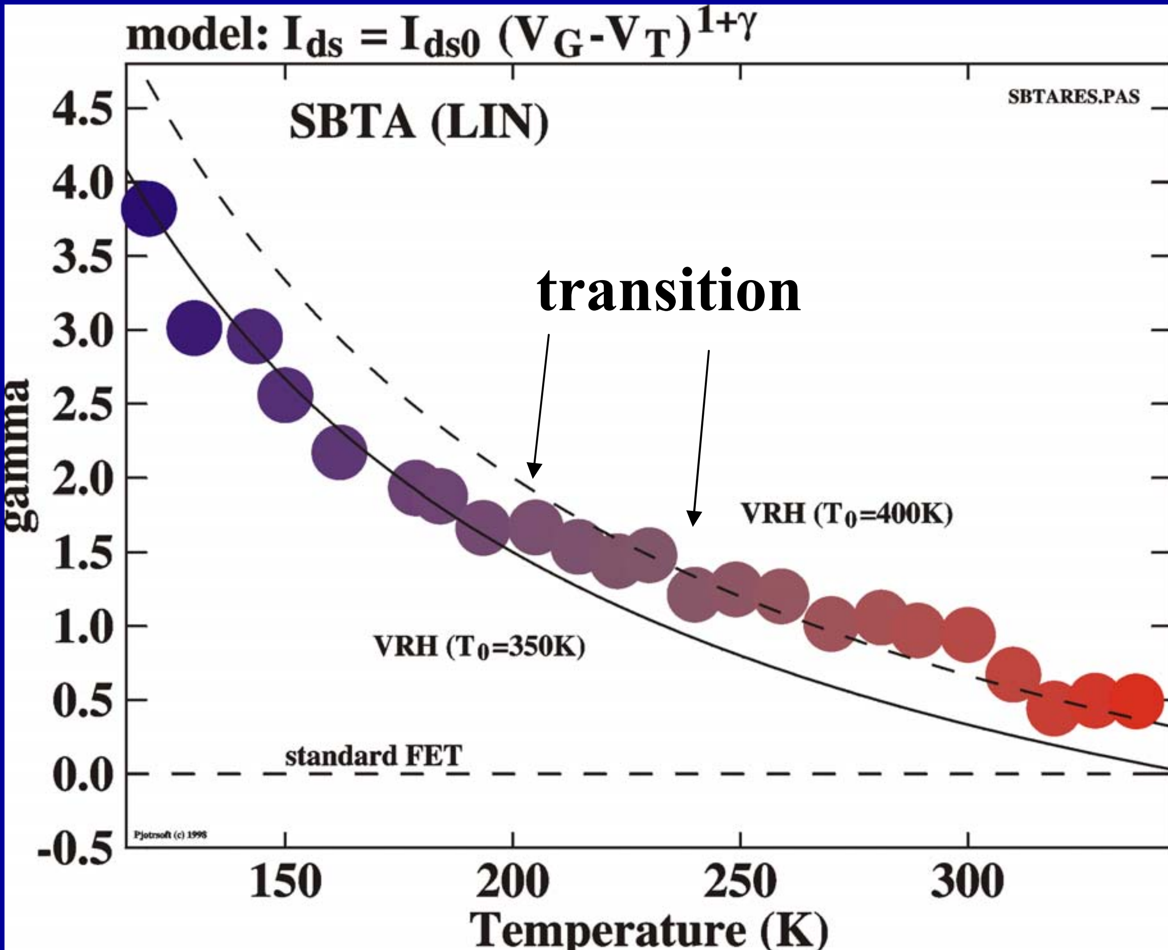


^{10}Log-^{10}Log plot.

Slope yields γ.

Corrected for V_T.

Comparison to VRH/MTR model

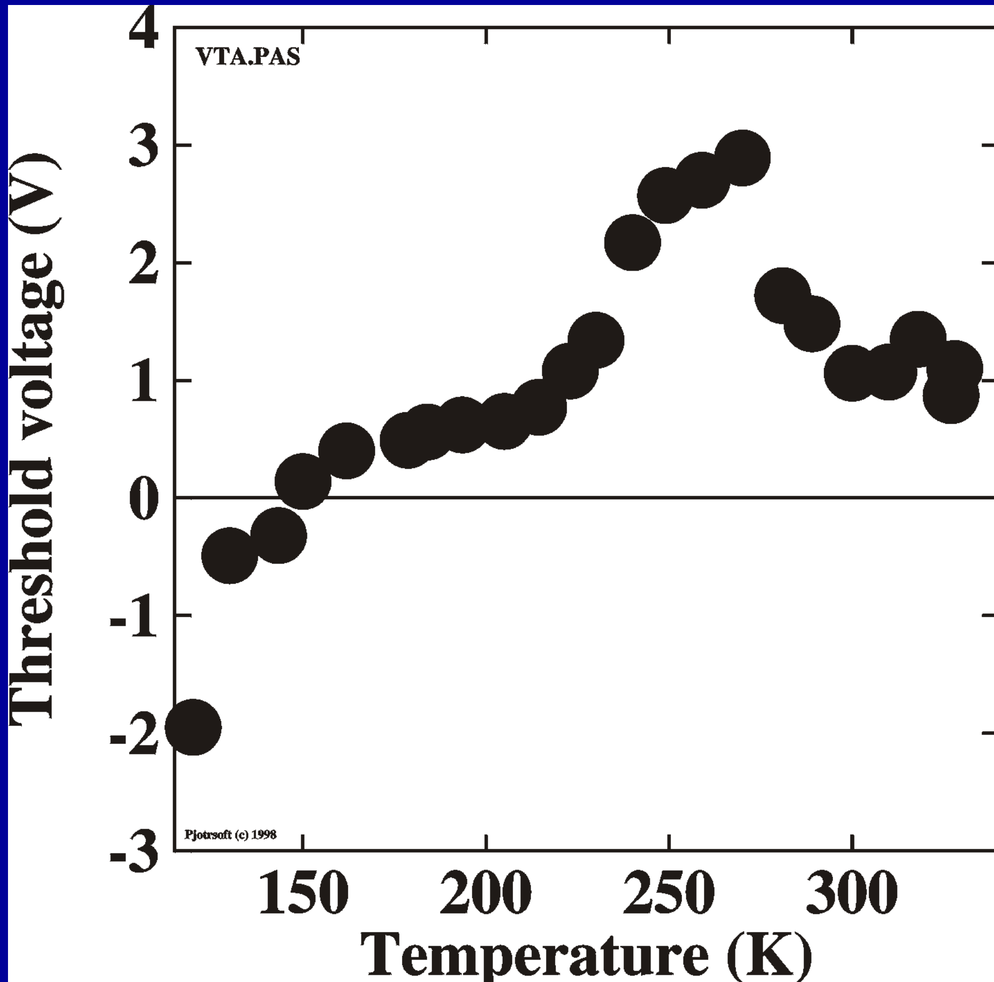


Model good for T<200 K (T_0 = 350 K)

Model good for T>240 K (T_0 = 400 K)

(phase) transition?

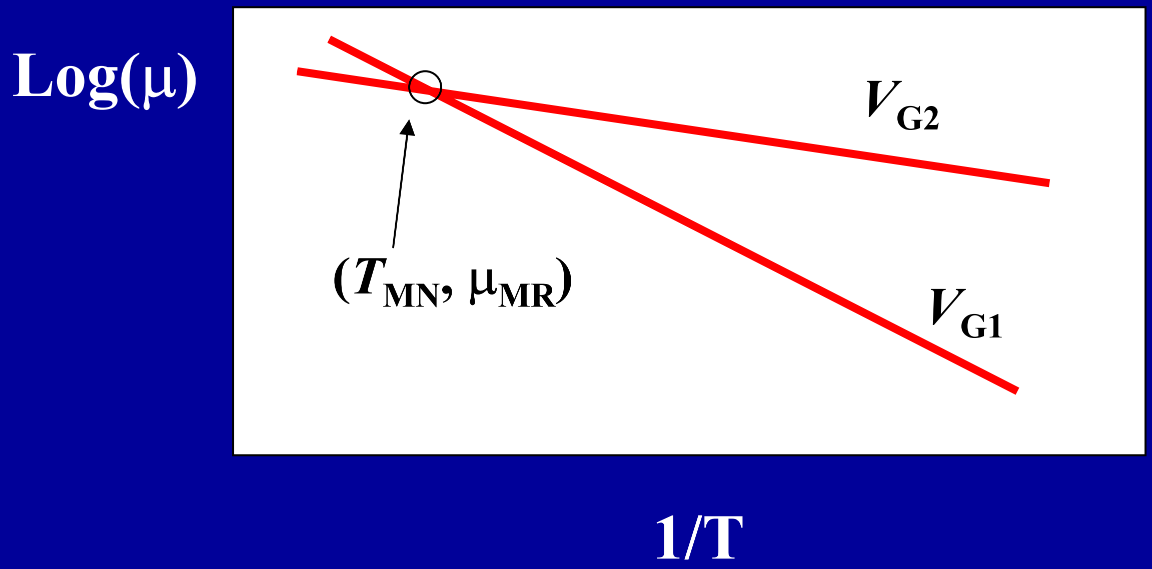
Threshold voltage shift



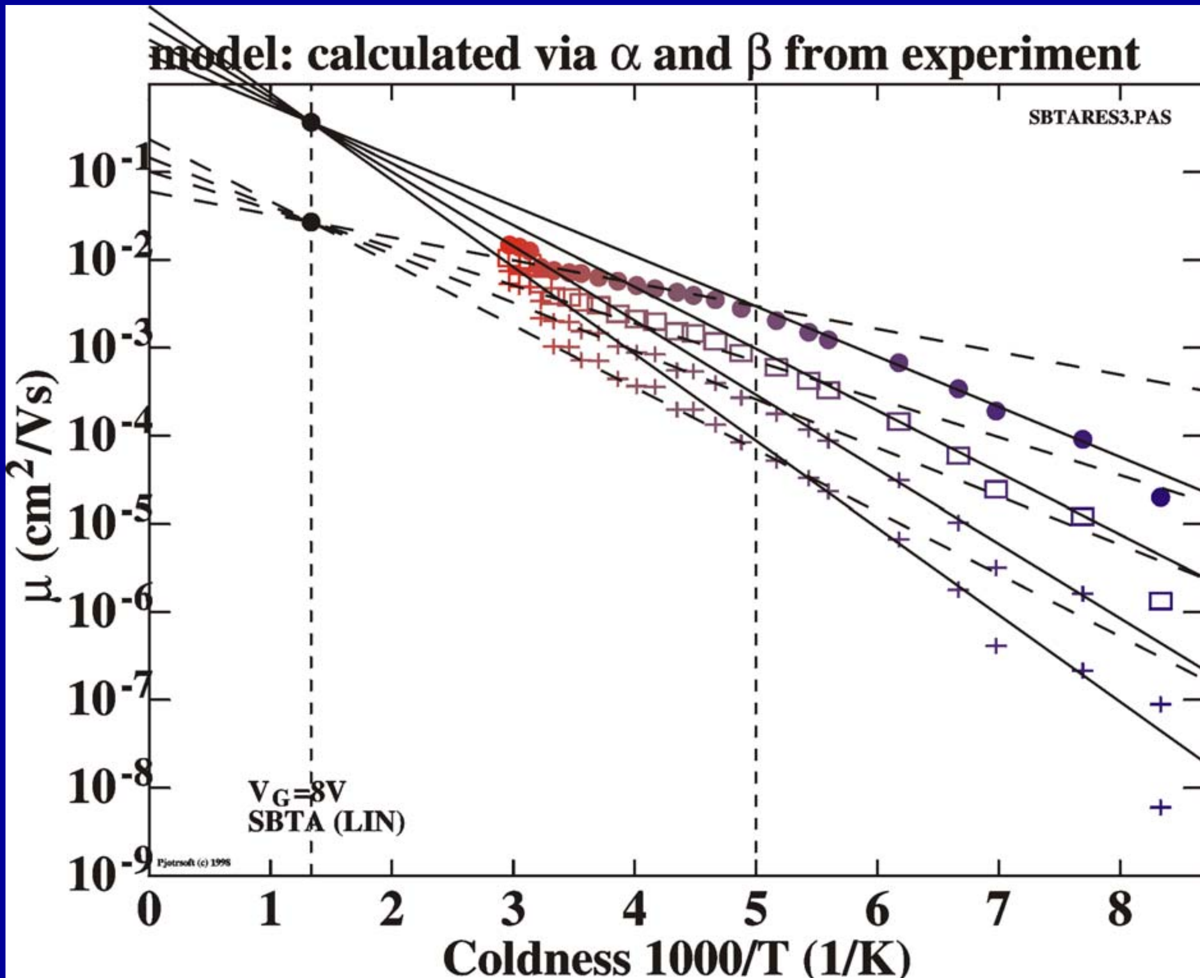
Simultaneously observed a threshold voltage shift

Meyer-Neldel rule

The Meyer-Neldel rule is an empirical rule, stating that the as-measured mobility, when plotted in an Arrhenius plot, for each gate voltages lies on a line and this line always points to the same "magical" point, (T_{MN}, μ_{MR}).

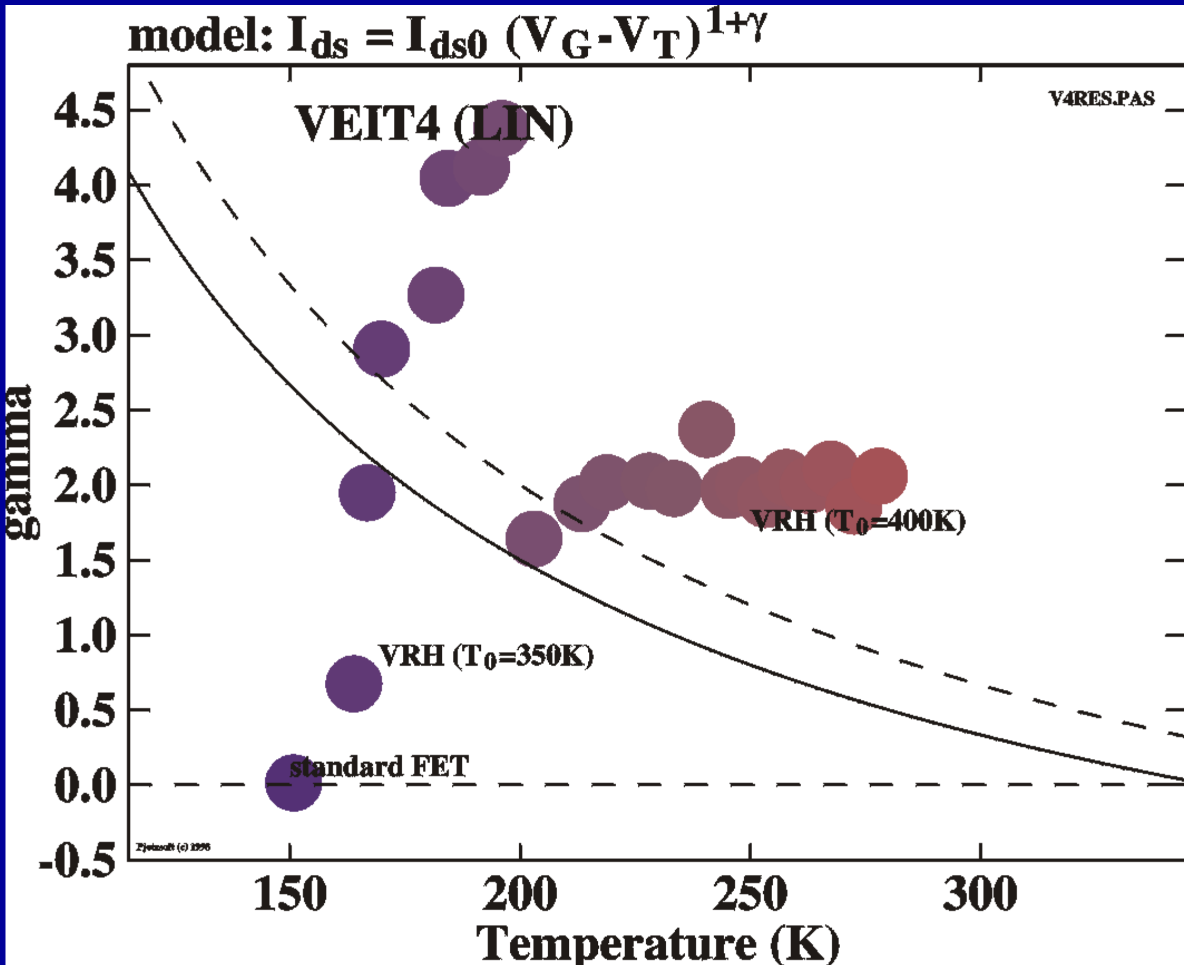


Meyer-Neldel for T6



MNR holds, with a phase transition at 200 K

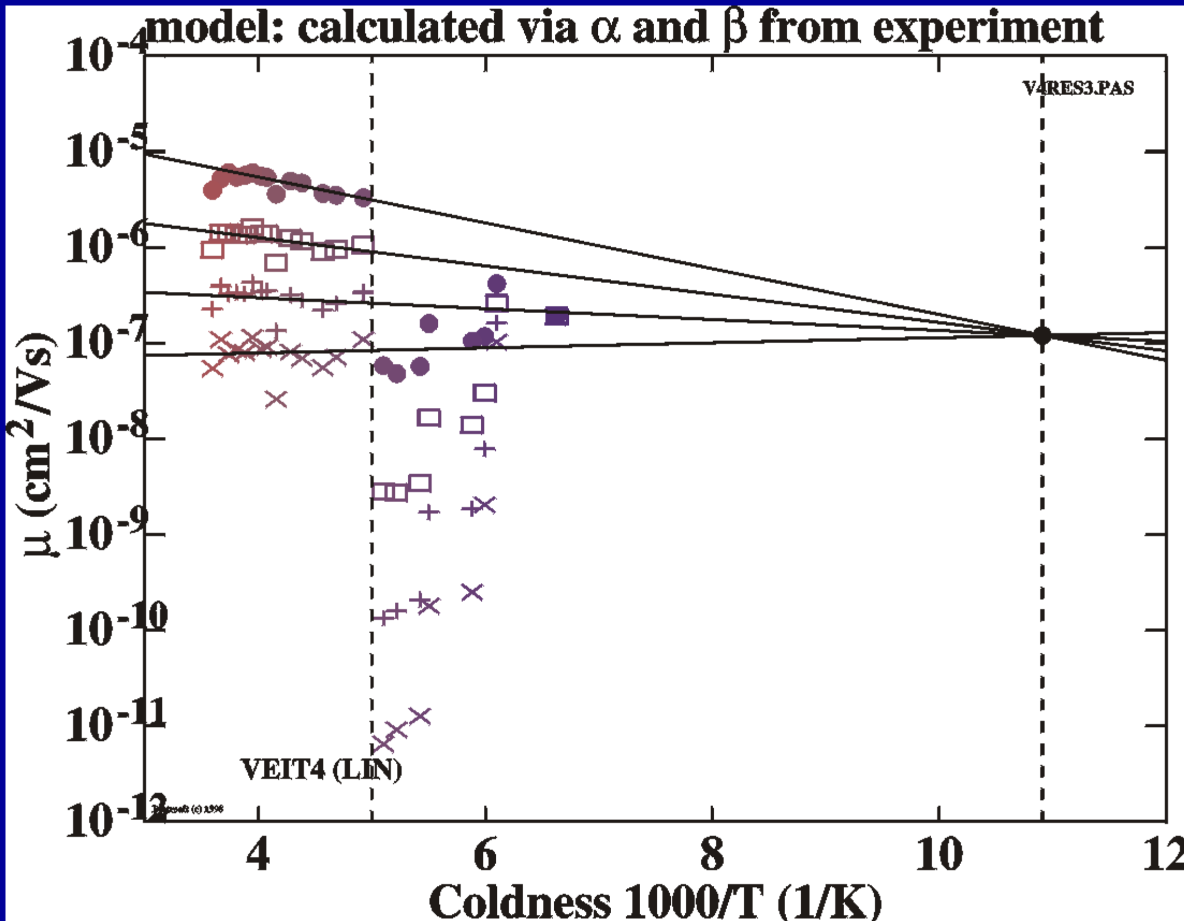
Nano FET, MTR/VRH analysis



Irregular MTR/VRH analysis.

Sample changes during heating?

Nano FET Meyer-Neldel Rule



Dramatic phase transition at 200 K.

Conclusions

• Failure of the VRH/MTR theory, which cannot adequately describe the behavior of γ as a function of temperature.

• Meyer-Neldel rule is still valid for these samples.

• Phase transition of the device at 200 K in the nano-FET and phase transition trajectory 200-250 K for micro-FET.

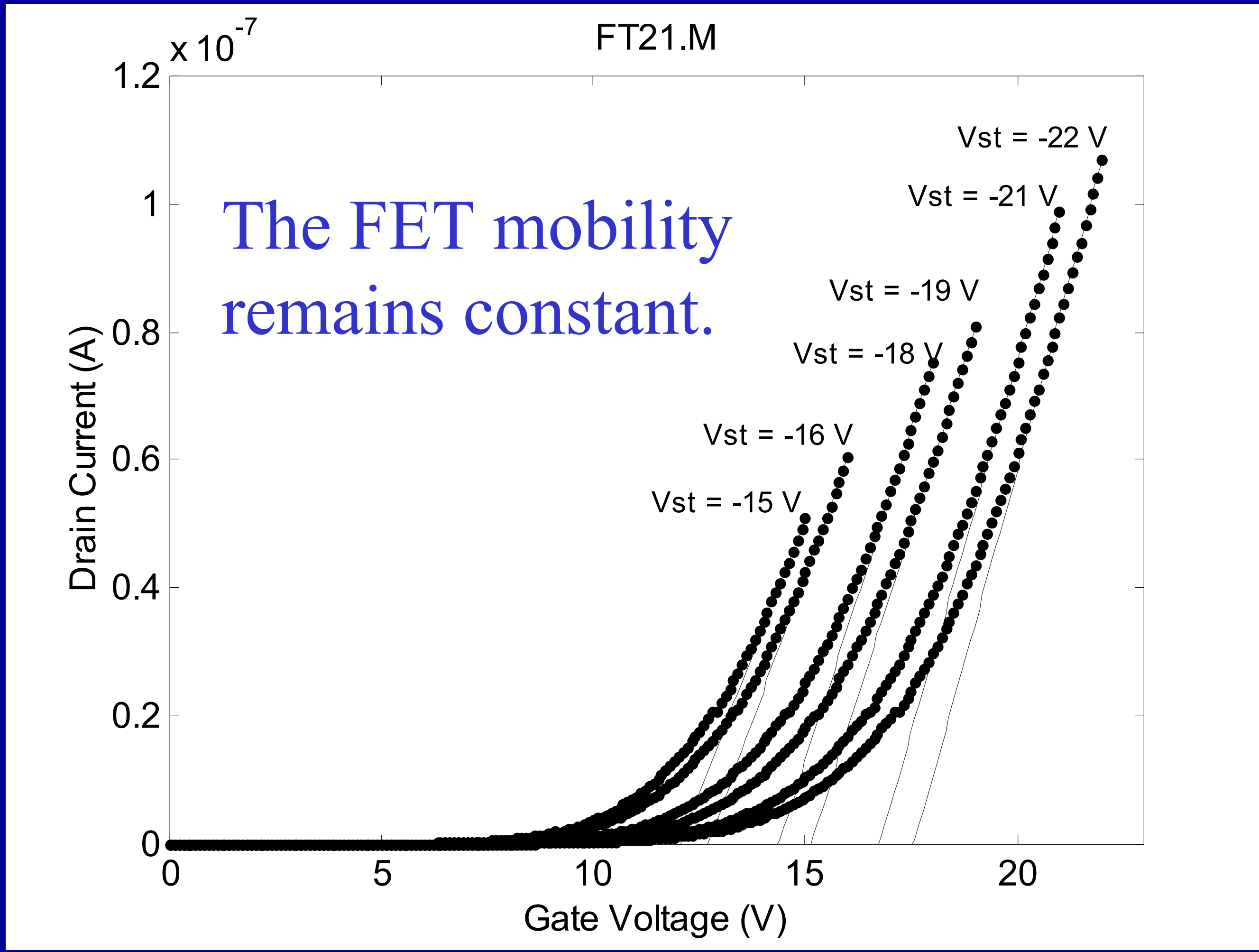
Meta-stability, a review

Transistors based on polycrystalline organic materials are meta-stable in a threshold-voltage shift upon prolonged gate voltage stress.

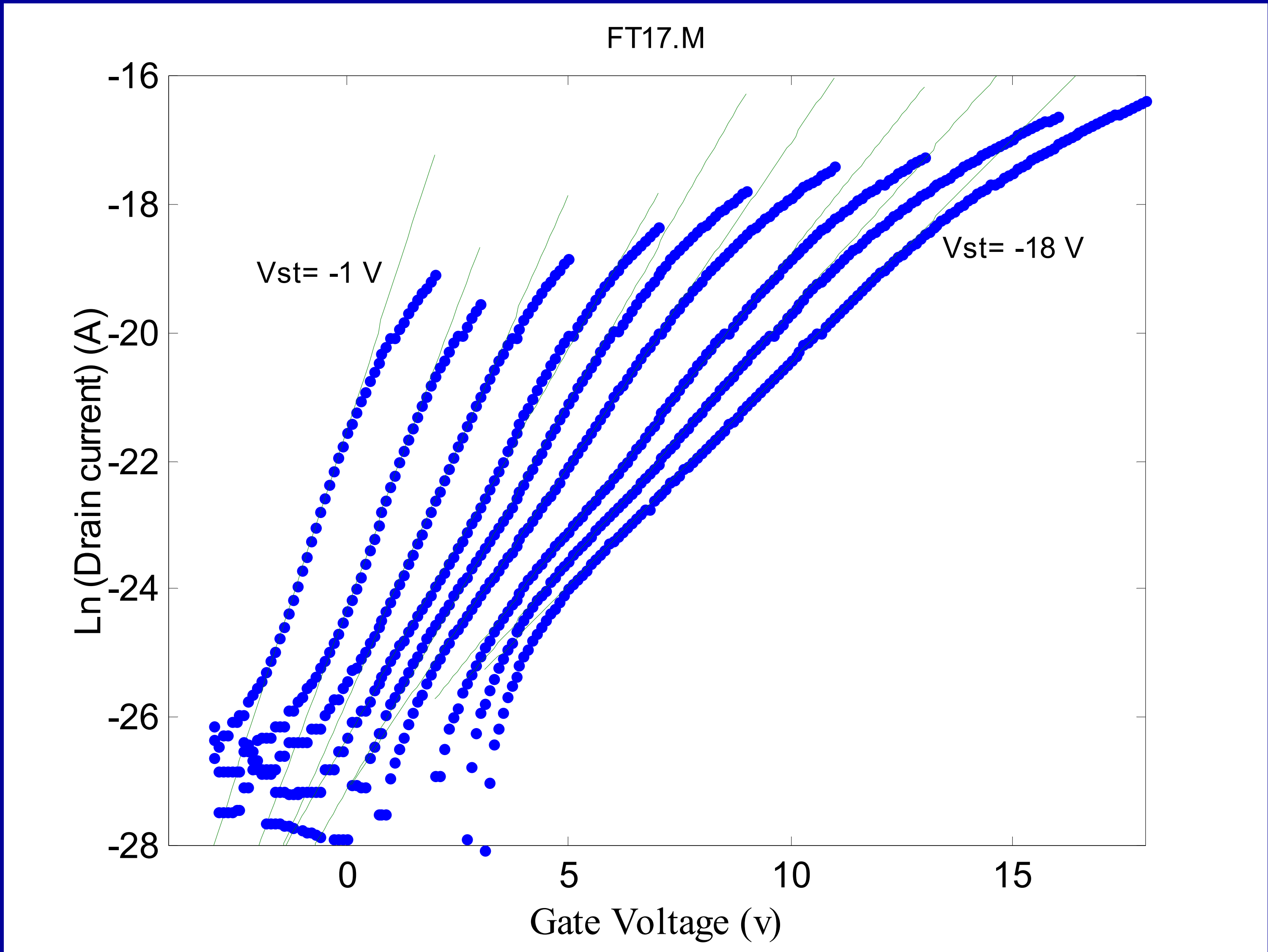
The instability:

- **does not depend on the insulator**.
- **depends on environmental variables, and surface dielectric treatments.**
- **Does not affect the FET mobility**.

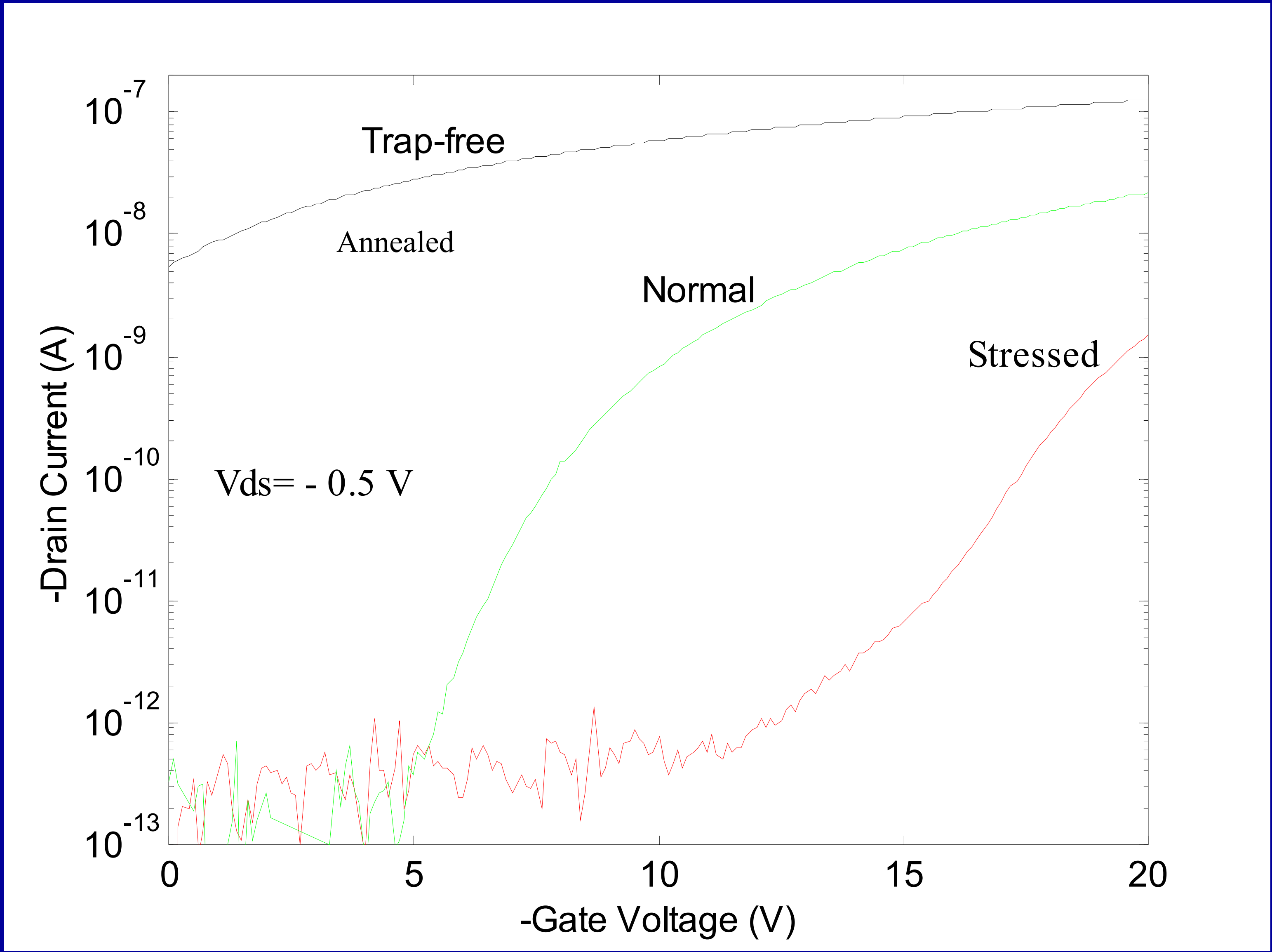
Threshold-voltage shift upon prolonged gate voltage stress.



The subtreshold slope changes with stress



There are three different meta-stable states.



What it is the kinetics of the relaxing and stressing processes ?

Annealed

Gently heat

+

V_G positive

(1)

Normal

Prolonged

V_G negative

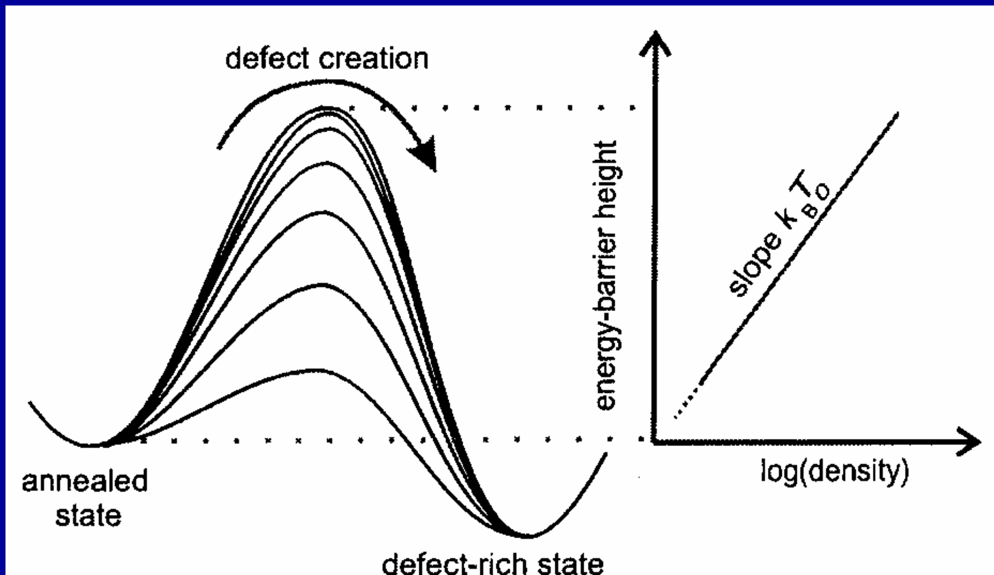
(2)

Stressed

We have to study:

- **Time dependence**
- **Voltage dependence**
- **Temperature dependence**

Thermalization-energy concept



This distribution of energy barriers D(E*)* can account for the observed no exponential kinetic behaviour

After a time *t* at a temperature *T*, all possible defect creation sites with $E \leq kTln(\nu t)$ will have converted into defects

A thermalization energy can therefore be defined by $E_{th}=kTln\ (\nu t)$ where ν is the attempt to escape frequency.

Stretched hyperbola function

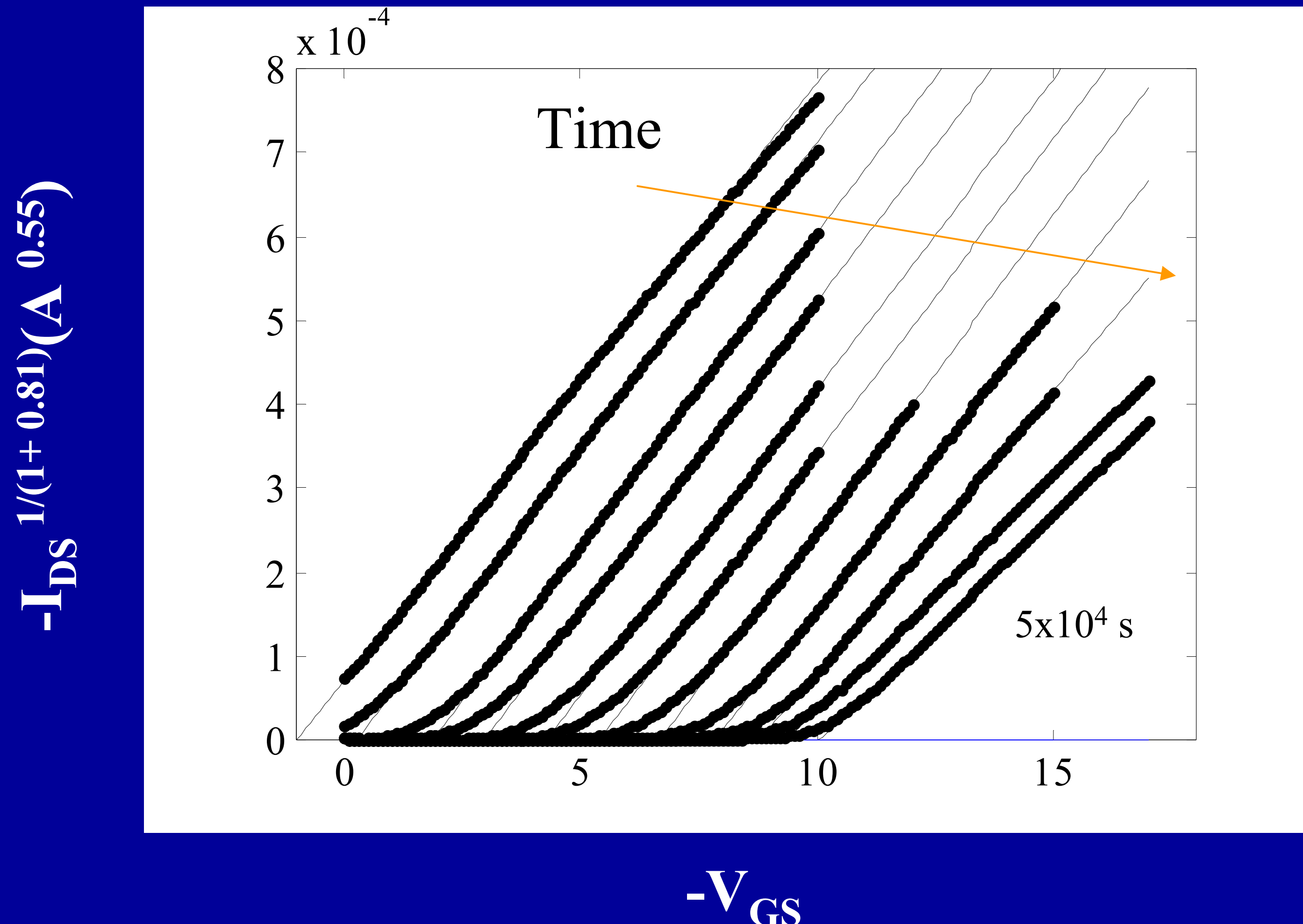
$$\frac{V_t - V_t^{ini}}{V_g - V_t^{ini}} = 1 - \frac{1}{\left(\exp\left\{\frac{E_{th} - E_A}{k_B T_o}\right\} + 1\right)^{\frac{1}{\alpha - 1}}}$$

This equation describes dispersive defect creation thermally activated with an exponential distribution of barrier heights, and a superlinear (α) dependence on the band-tail carrier density.

E_A is the mean activation energy for defect creation.

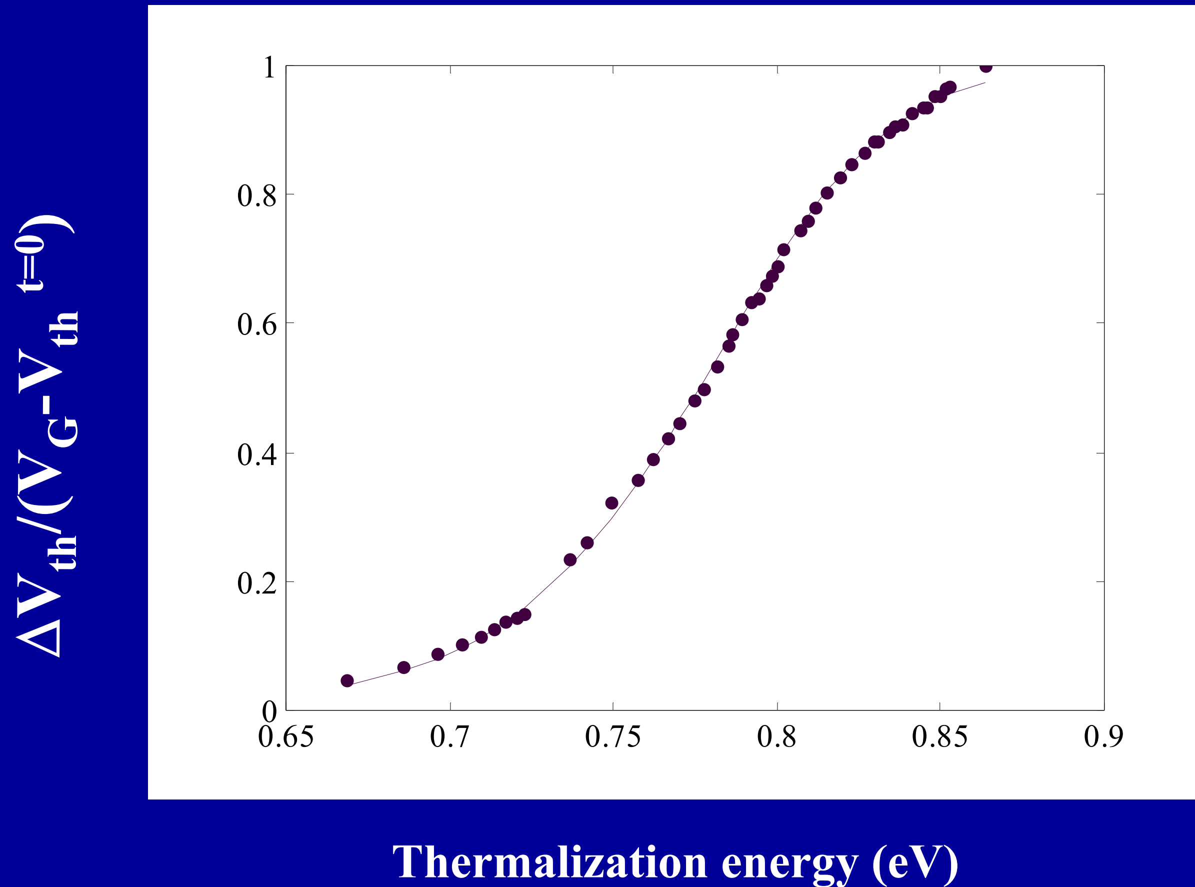
$k_B To$ is the slope of the barrier height distribution.

Evolution of the linear transfer curves with increasing stress time



Curves plotted as $I_{DS}^{1/(1+\gamma)}$ vs. V_{GS}. With γ=0.81. Vg=-10V .

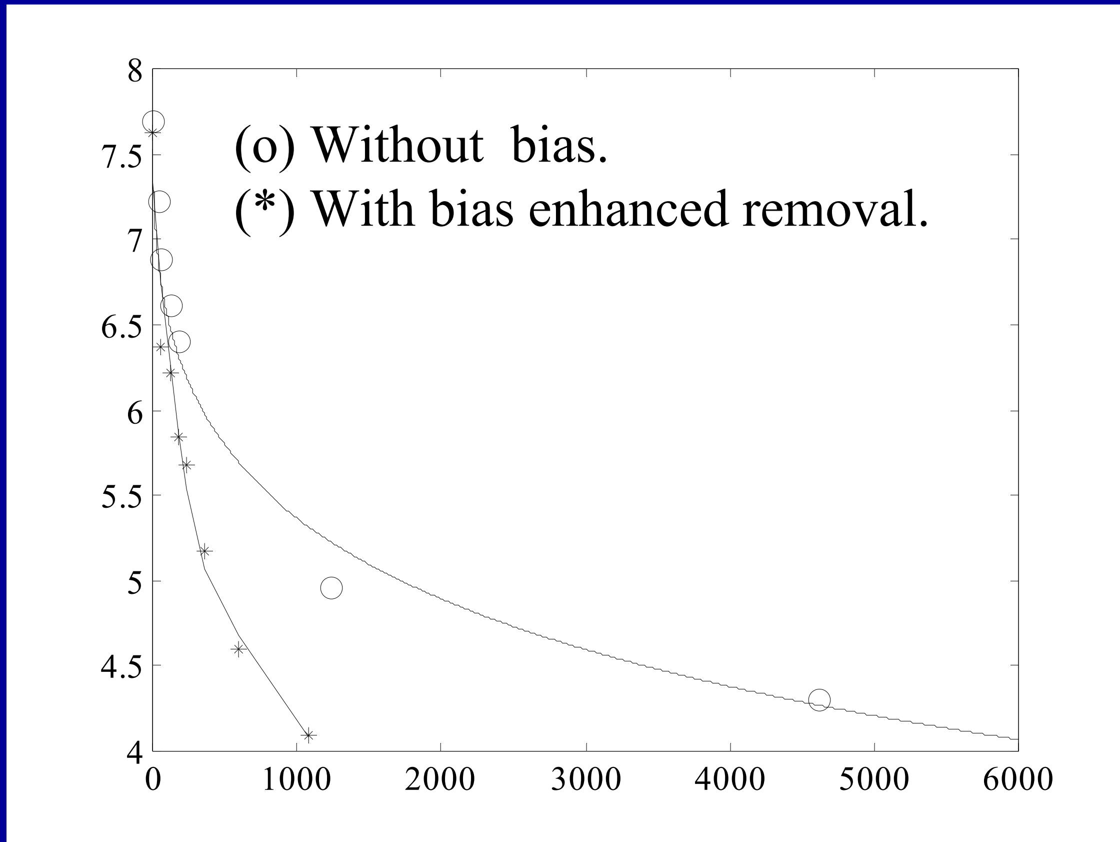
Relative threshold-voltage shift versus thermalization energy E_{th}



E_A(eV)	$K_B T_0$(meV)	α	ν_0 (Hz)
0.807	**35**	**1.5**	**10^9**

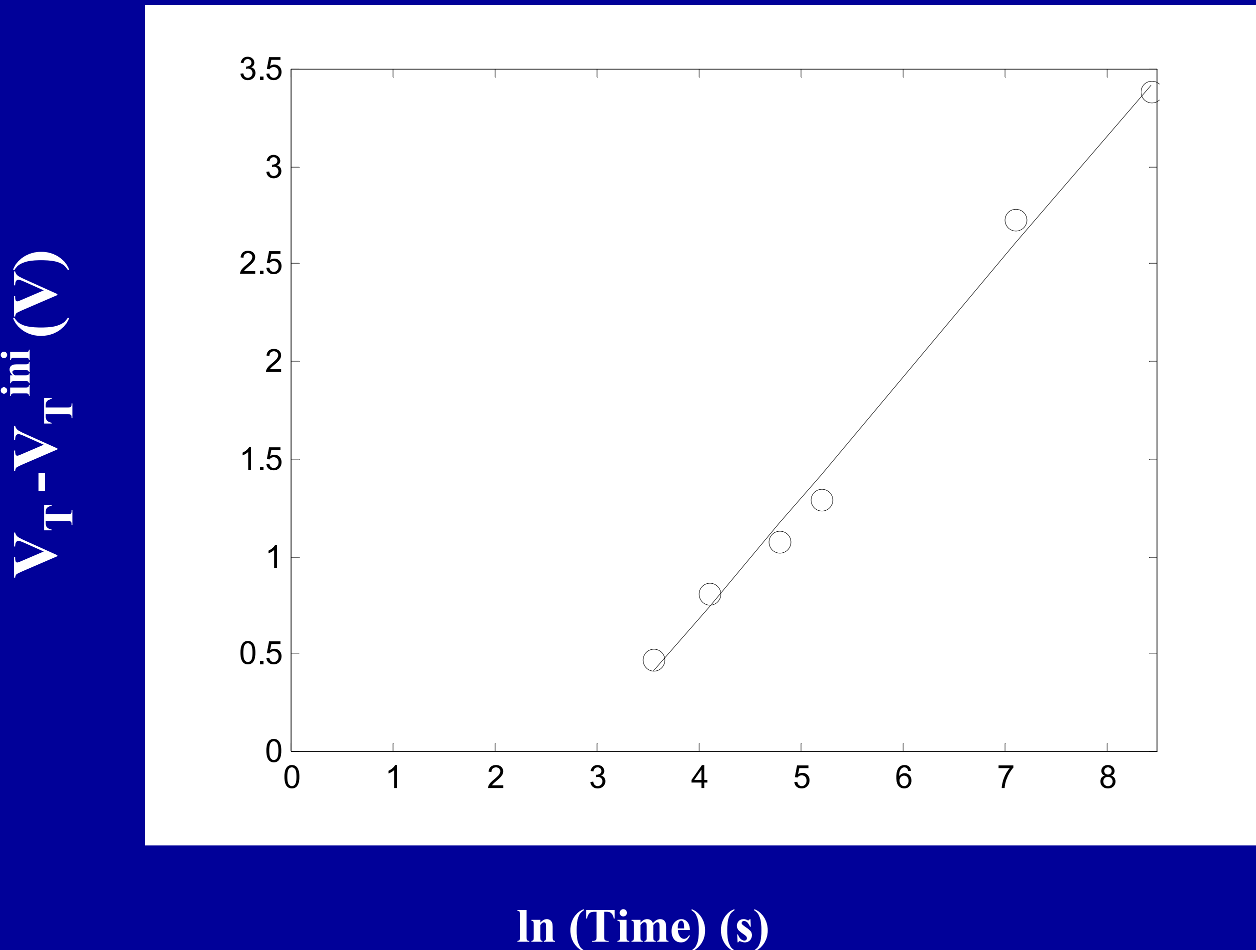
Table I. Fitting parameters are α and $k_B To$. ν_0 and α can be determined independently.

Defect removal



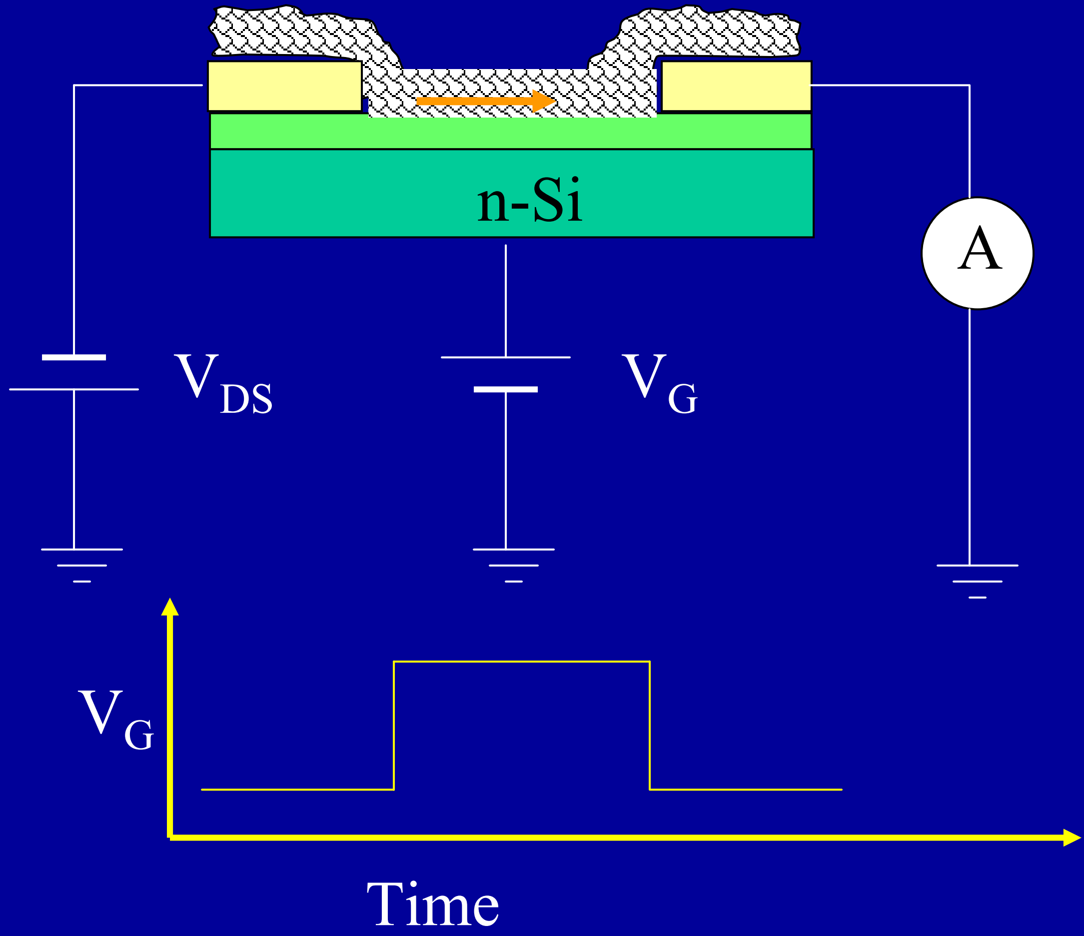
Time (s)

Decrease of the threshold voltage with time, (o) without any bias applied to the device, (*) with +10V applied in the gate.

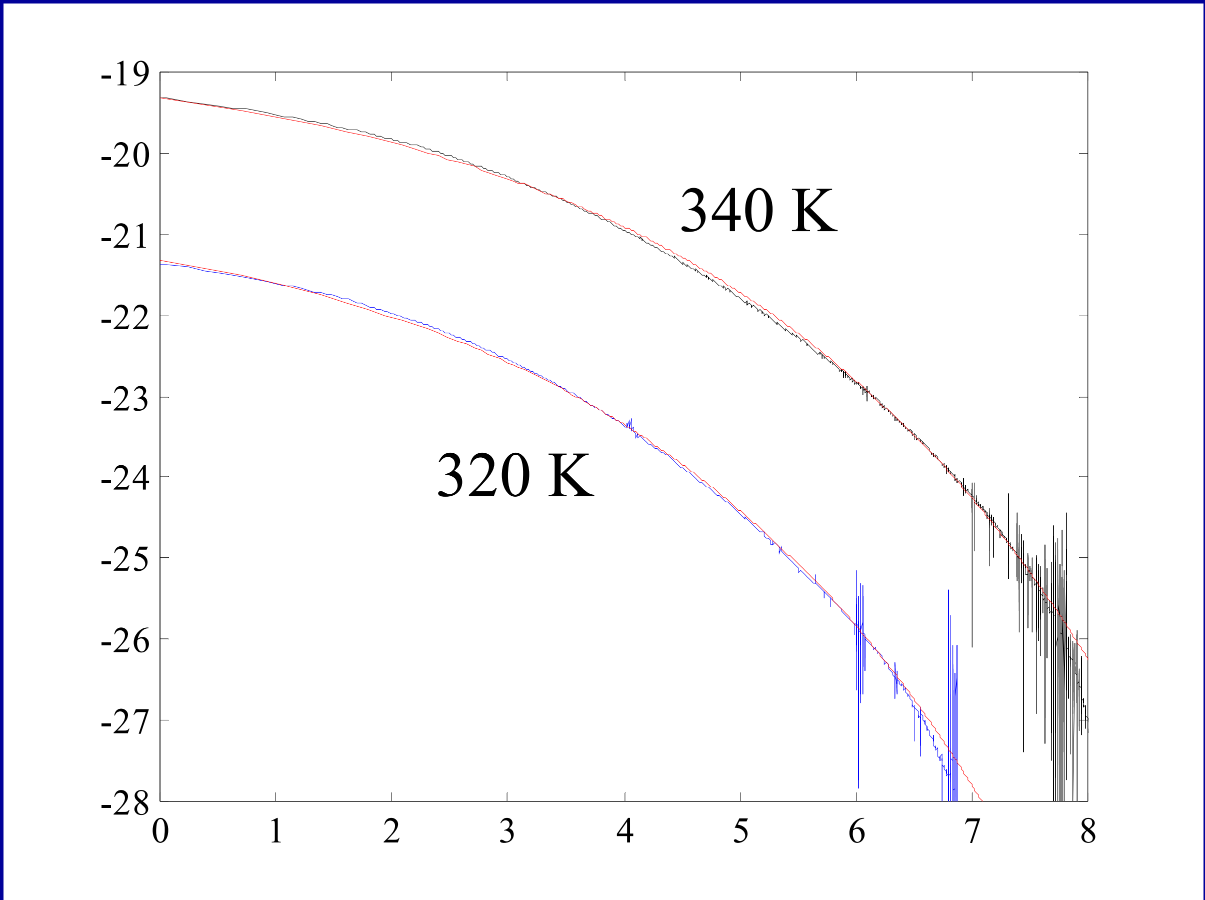


Decrease of the threshold voltage with time, without bias applied to the device.

I_{DS} transients upon gate voltages changes follows a streched exponential beaviour



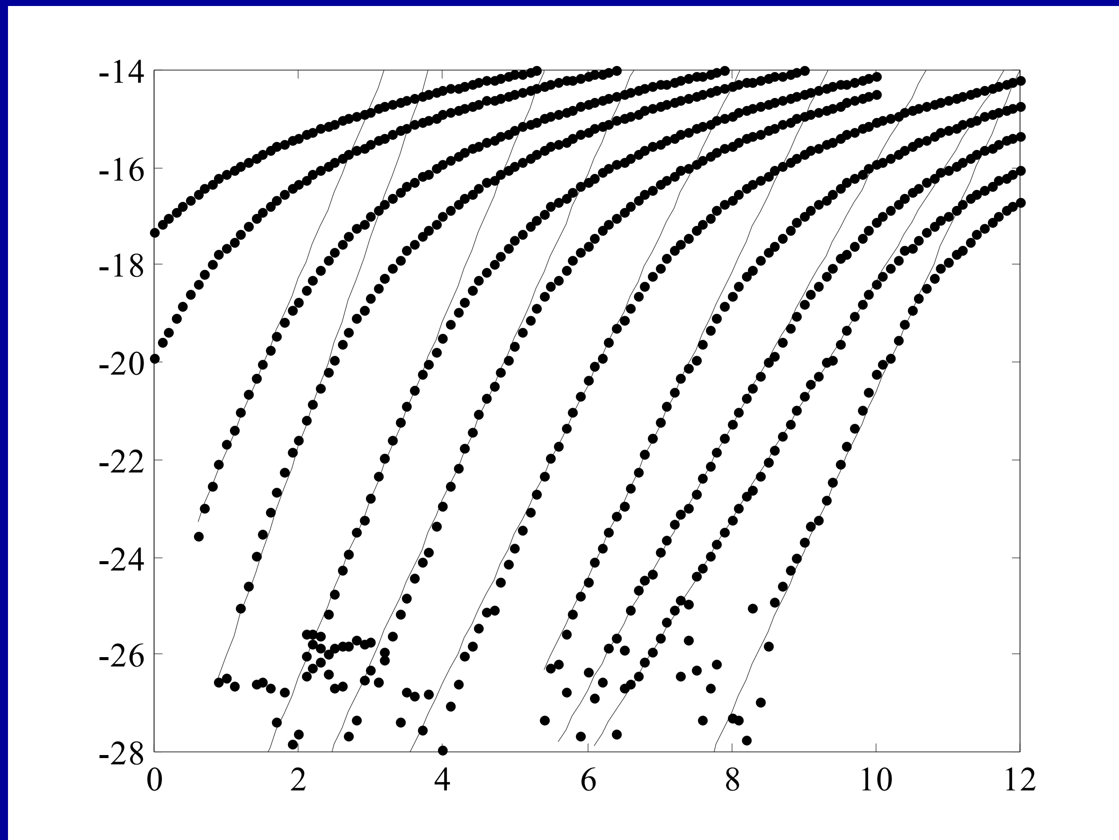
$$I_{DS} = I_0 \exp\left[-\left(\frac{t}{\tau}\right)^{\beta}\right]$$



$$I_{DS} = I_0 \exp\left[-\left(\frac{t}{\tau}\right)^{\beta}\right]$$

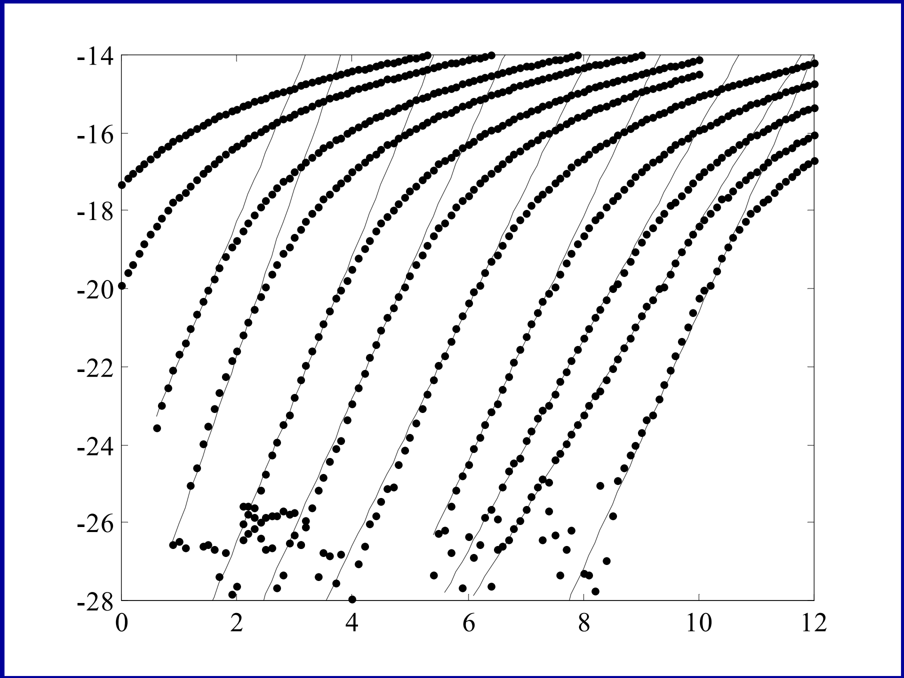
T (K)	τ (s)	β
340	**3.48**	0.30
320	**1.97**	0.31

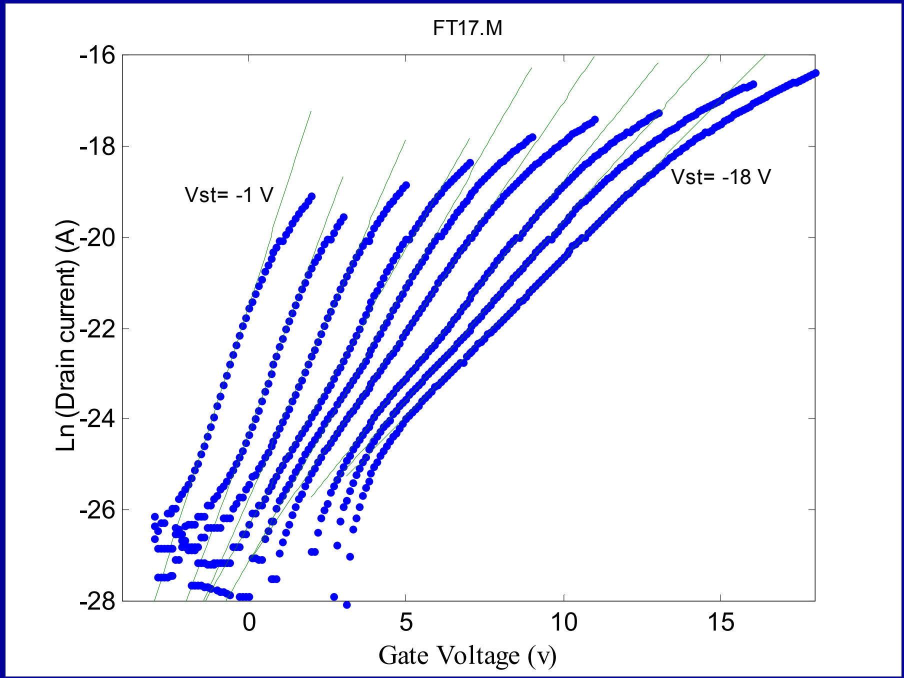
Time dependence of the subthreshold slope.



Evolution of the subthreshold swing with the stress time for a negative gate stressing voltage of 10V.

The effect of stressing in the subthreshold slope.

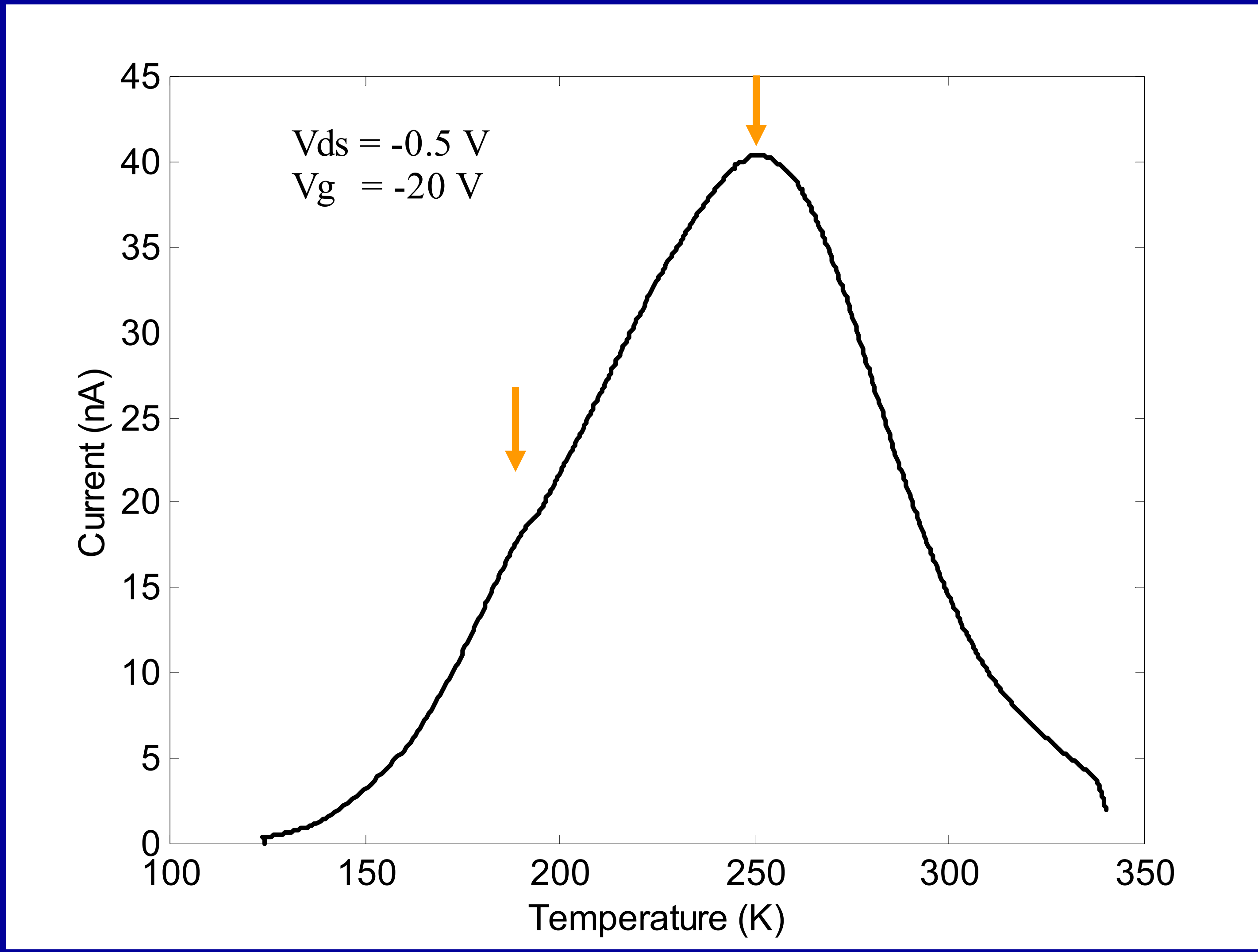




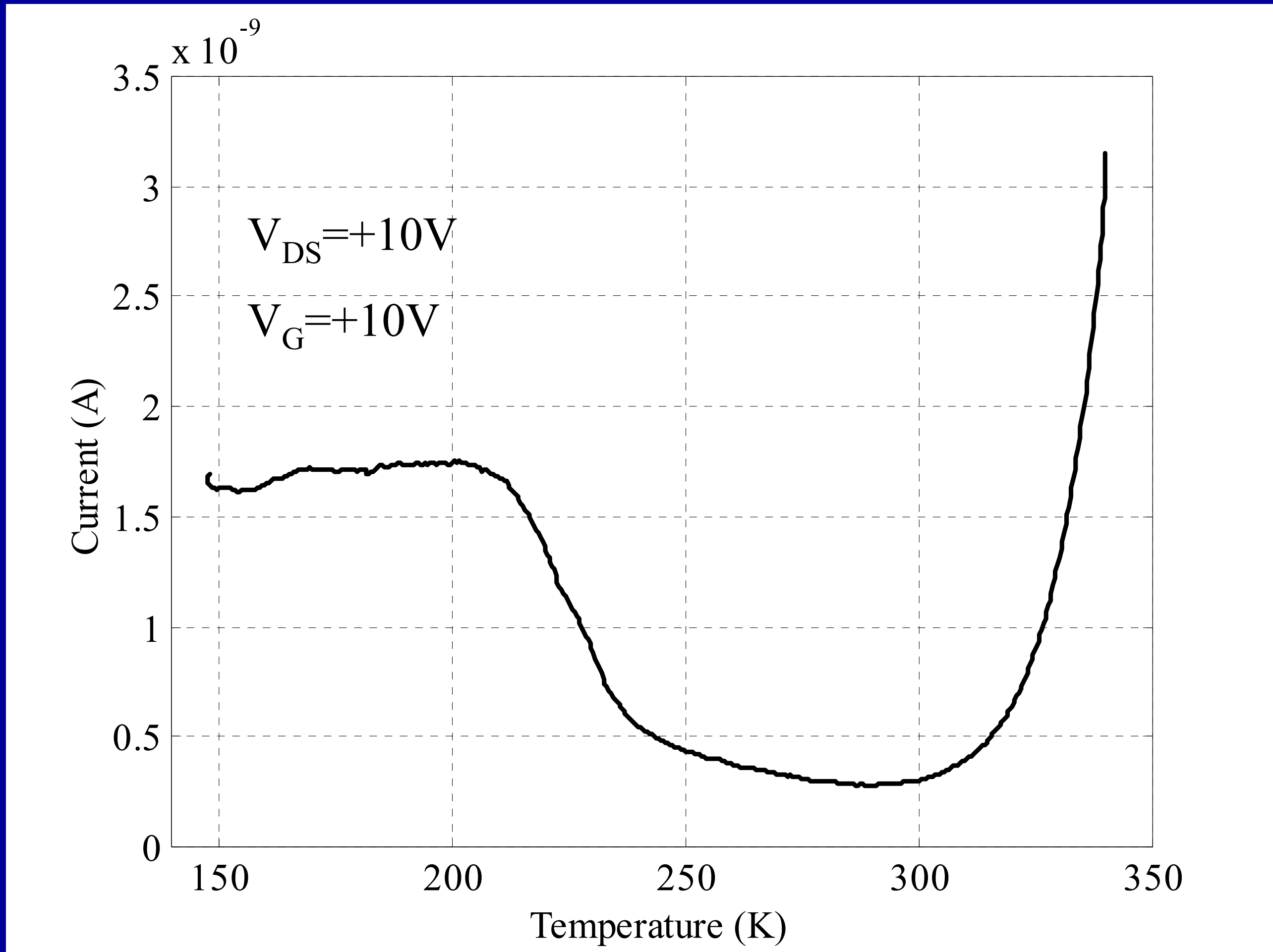
Stressing at constant voltage

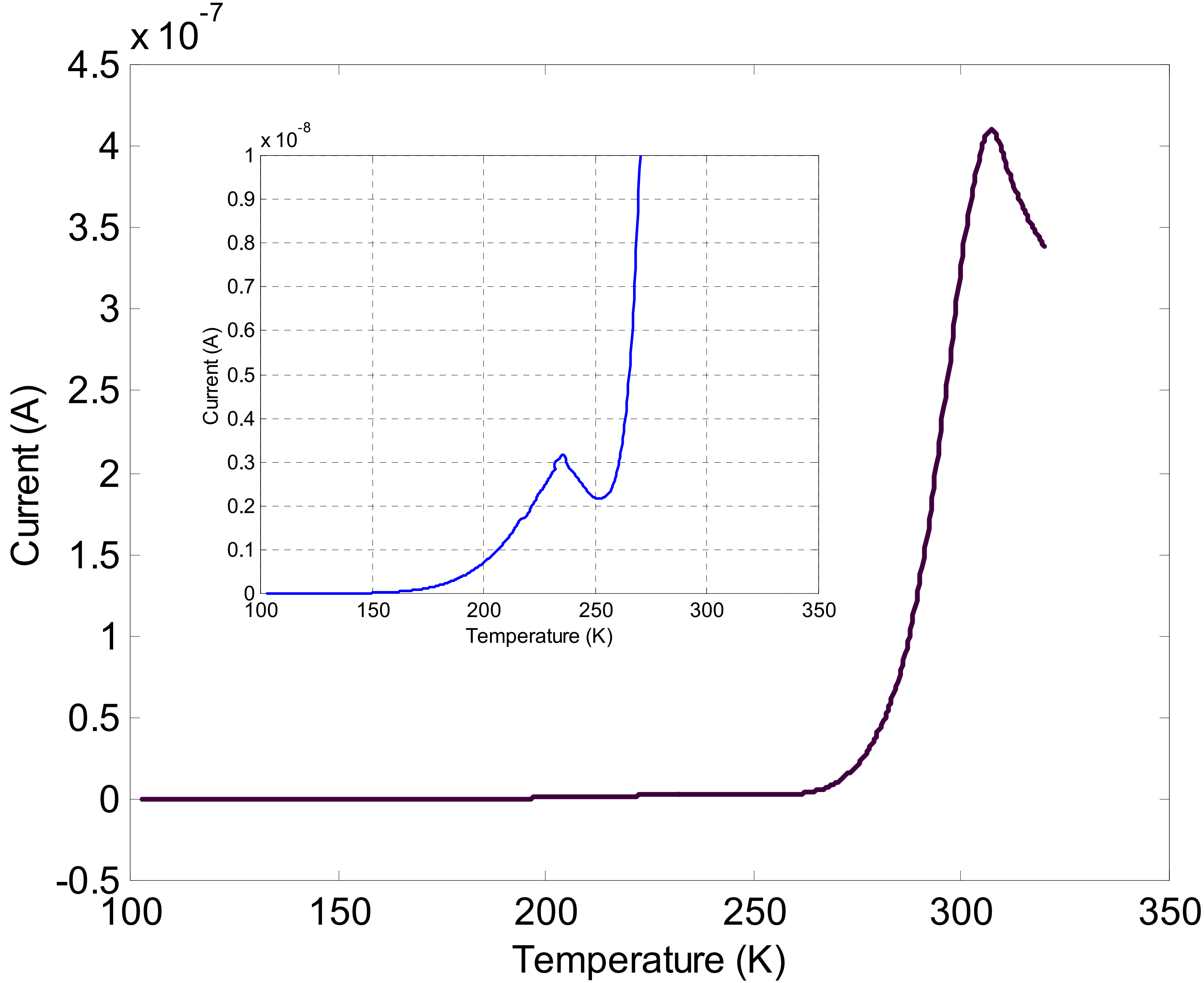
Stressing at different gate voltages

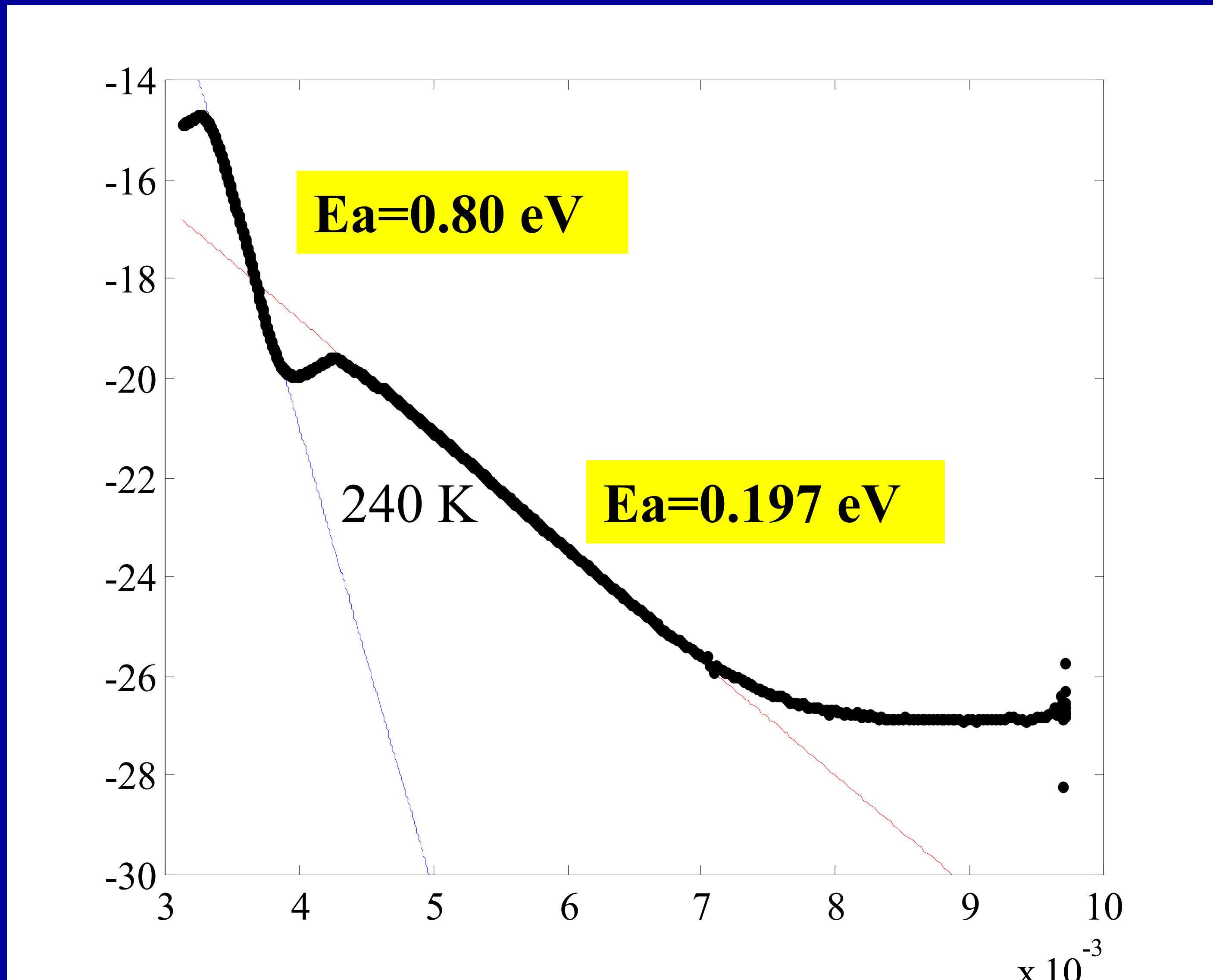
Temperature dependence



Temperature dependence

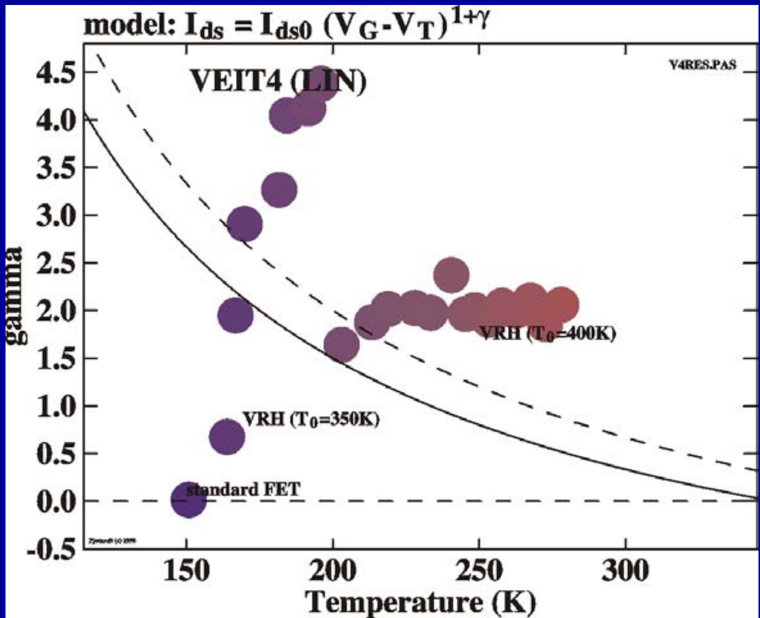


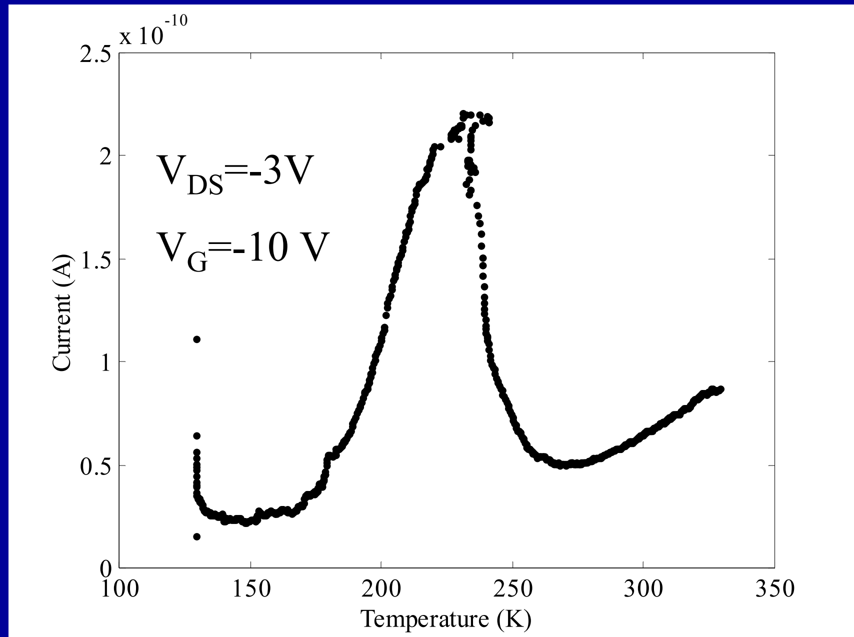

x 10^-7
4.5
4
3.5
3
2.5
2
1.5
1
0.5
0
-0.5
Current (A)
100
150
200
250
300
350
Temperature (K)
x 10^-8
1
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
Current (A)
100
150
200
250
300
350
Temperature (K)



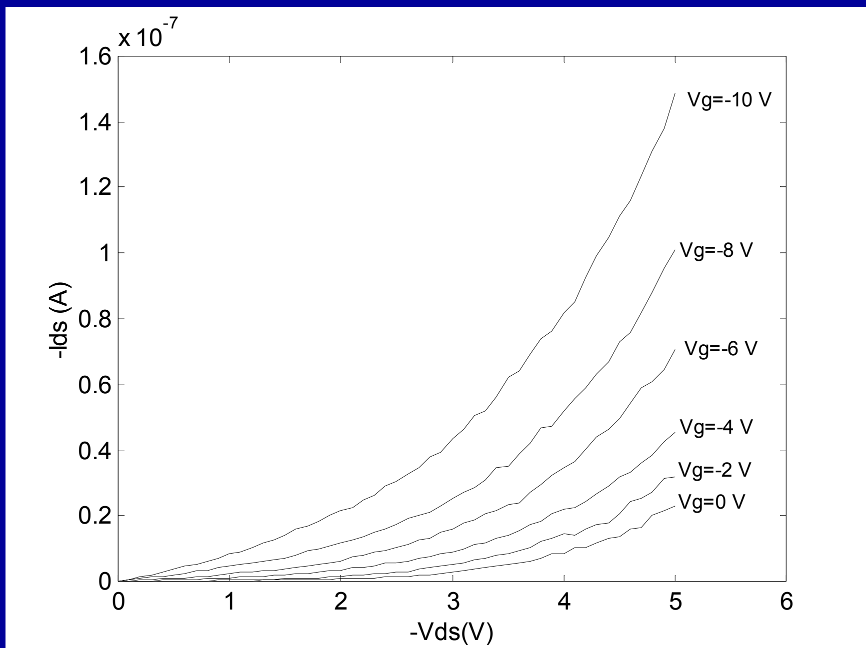
Ea=0.80 eV
Ea=0.197 eV
240 K
-14
-16
-18
-20
-22
-24
-26
-28
-30
3
4
5
6
7
8
9
10
x 10
-3

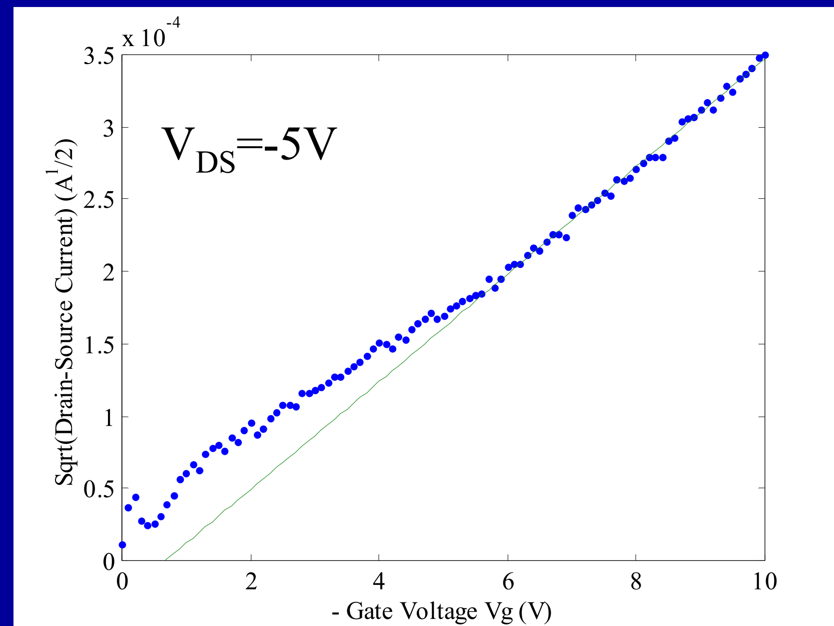
Temperature dependence (200 nm device)





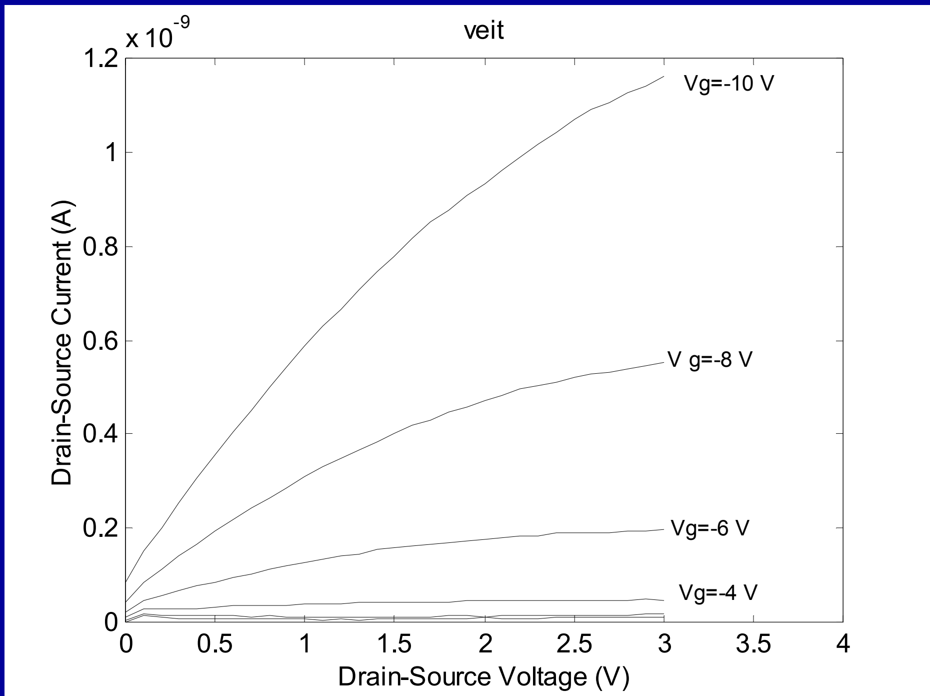
Characteristics of a 40 nm transistor

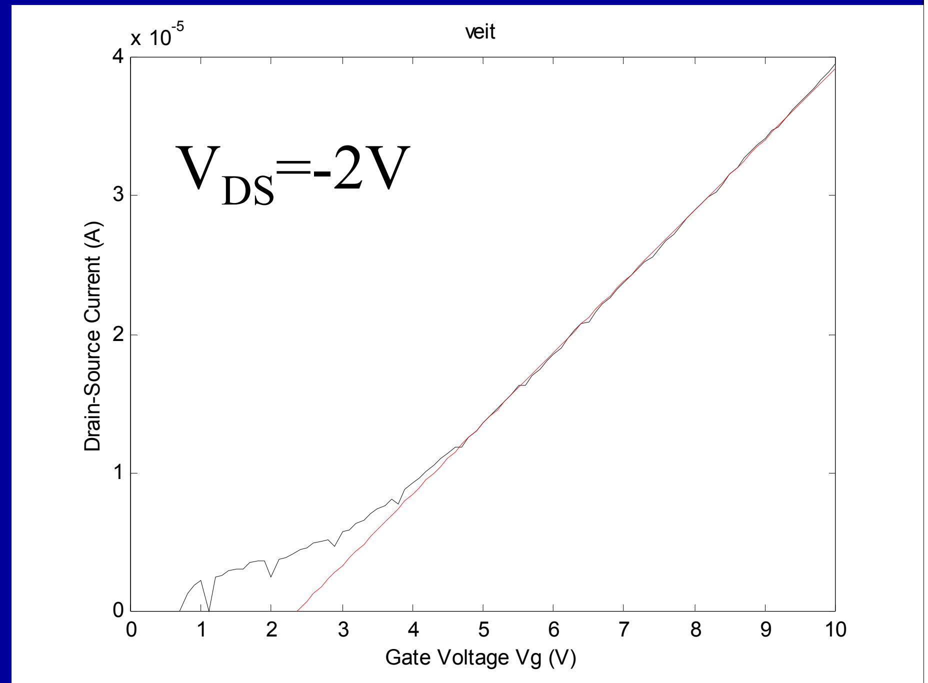




$\mu = 0.087\ Vcm^{-2}\ V^{-1}s^{-1}$

Characteristics of a 200 nm transistor





$\mu = 0.1\ \mathrm{Vcm^{-2}\ V^{-1}\ s^{-1}}$

Conclusions

•The γ parameter should be used to compare the performance of different devices.

•Major changes (charge transport and/or stress kinetics) at the temperatures of 200 K, 240-250 K and 310 K.

•The device metastability can be described by a stretched hiperbola or stretched exponential behaviour. Using this mathematical formalism, we can get a parameter (E_A) to characterize device stability.