Electrical characterisation of Transistors

Centre of Electronics Optoelectronics and Telecommunications, Faro, Portugal

Henrique Leonel Gomes and Peter Stallinga

Development of Novel Conjugated MOlecular NAnostructures by LIthography and their Transport Scaling Aspects (MONA-LISA)

Eindhoven, June 2002

Areas of research

- Semiconductor and device assessment.

  We mainly consider a wide range of experiments designed to measure essential parameters such as:

  - **Free carrier density**
  - **Field effect mobility**
  - **Donor and acceptor densities.**
  - **Deep level and interface state densities.**

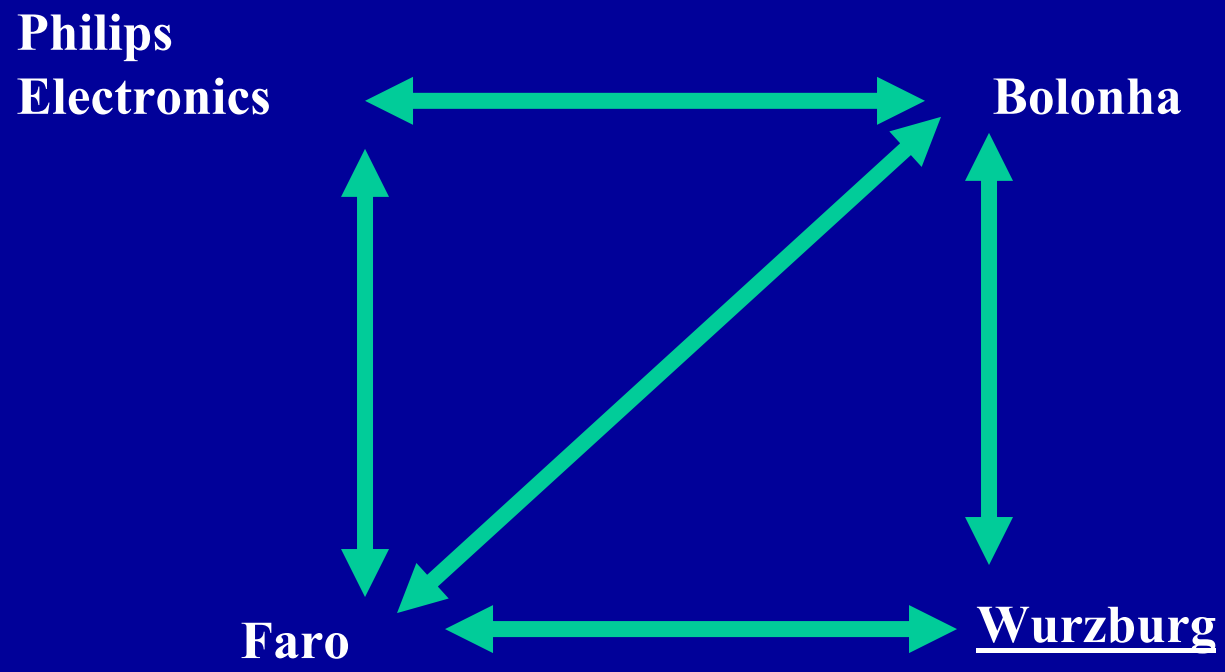
Outline

- Device performance.

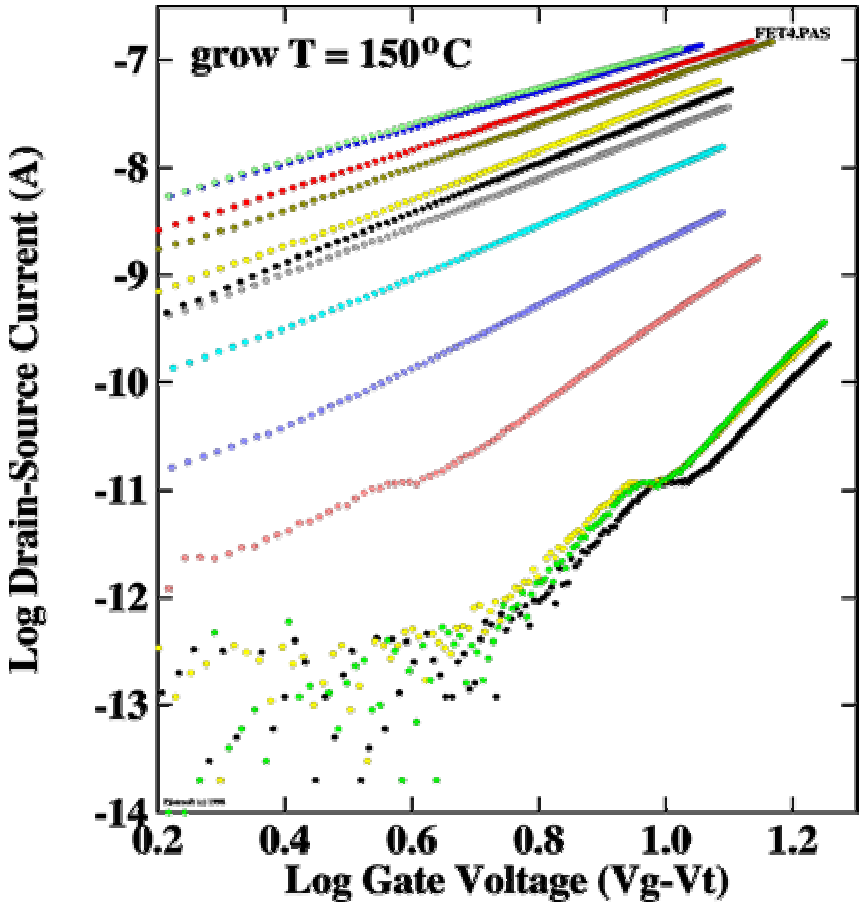
- Charge transport mechanisms.

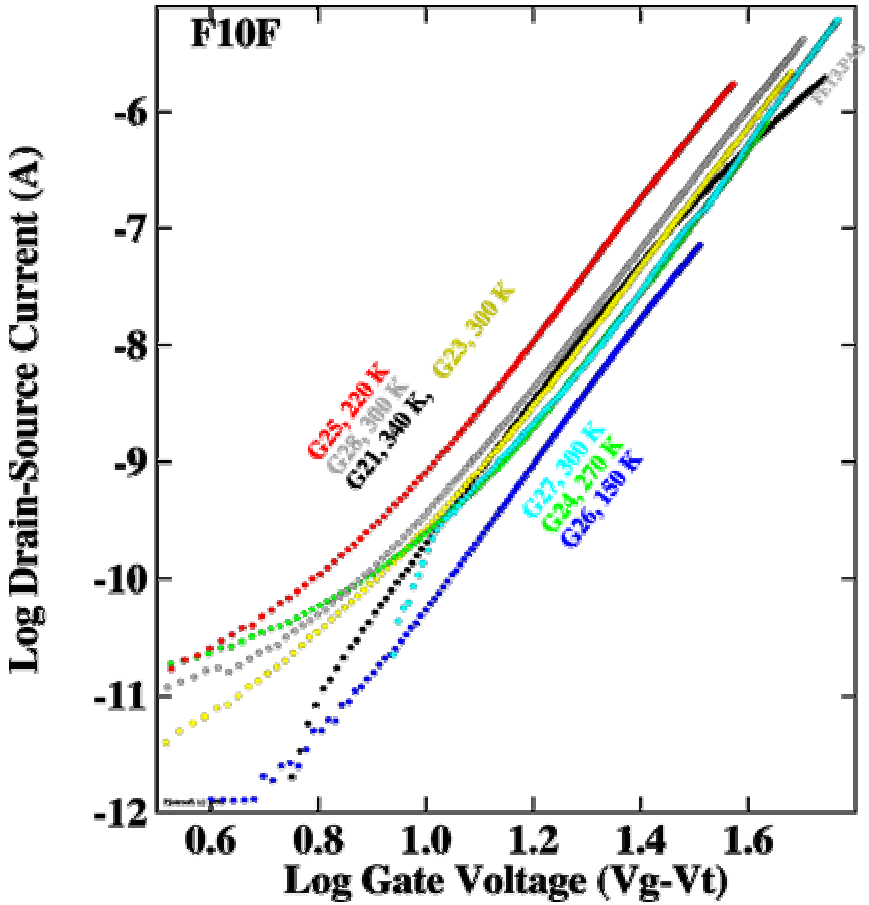
- Stability and reability issues
(effects of traps and interfacial problems).

Interactions with MONA-LISA Partners

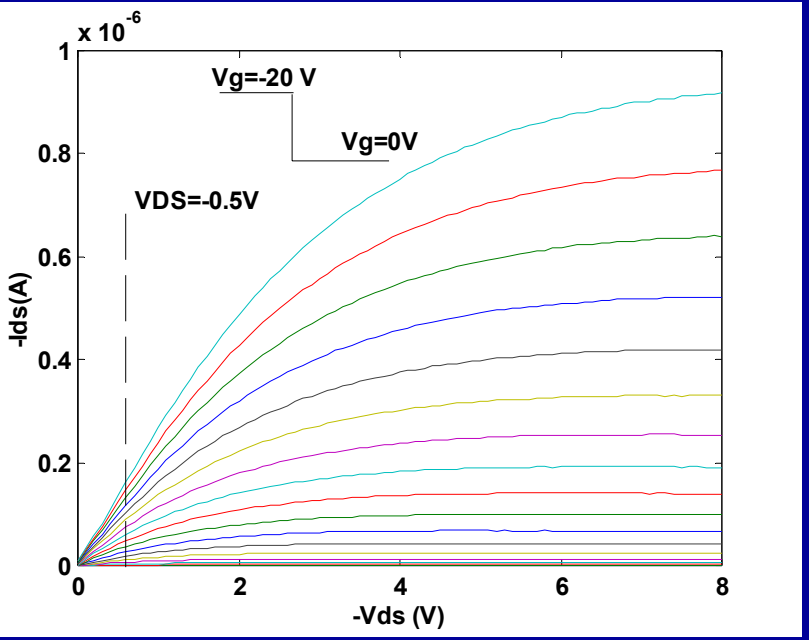


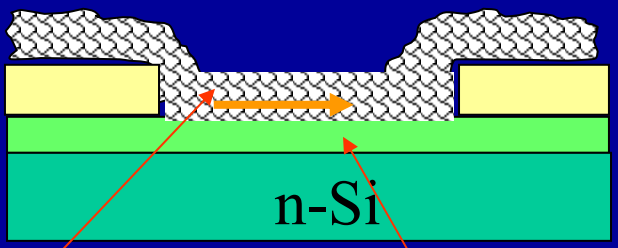
Charge transport mechanisms.





DLTS Experiments





Bulk traps $N_{bs}(E)$

Interface traps $N_{is}(E)$

$$S(t) = A_0 - A\sqrt{\frac{1}{1-\frac{N_T}{N_D}\left[1-\exp(-t/\tau)\right]}}$$

$$S(t) = A_0 - A\sqrt{1-\exp(-t/\tau)}$$

The transient has not an exponential decay

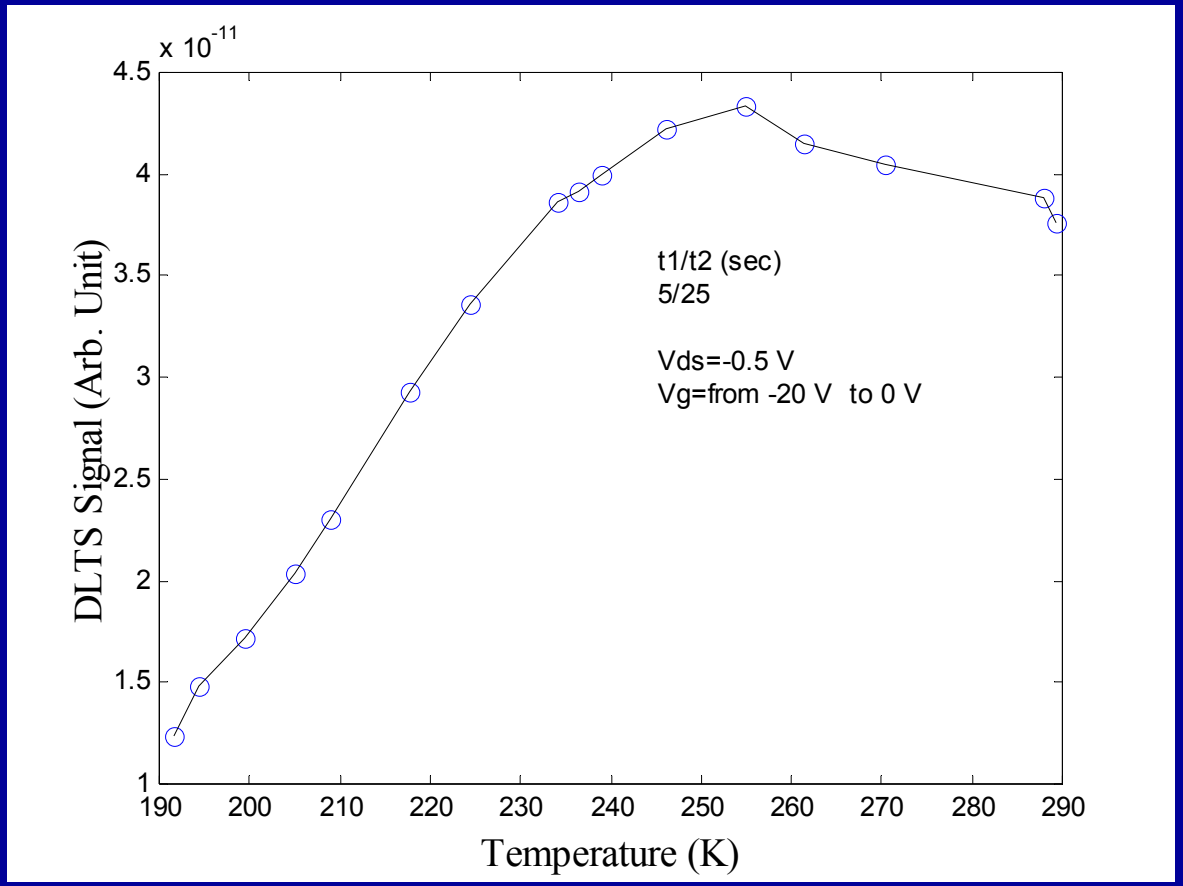
→

Overlap of responses times from several close traps.

Large density of traps.

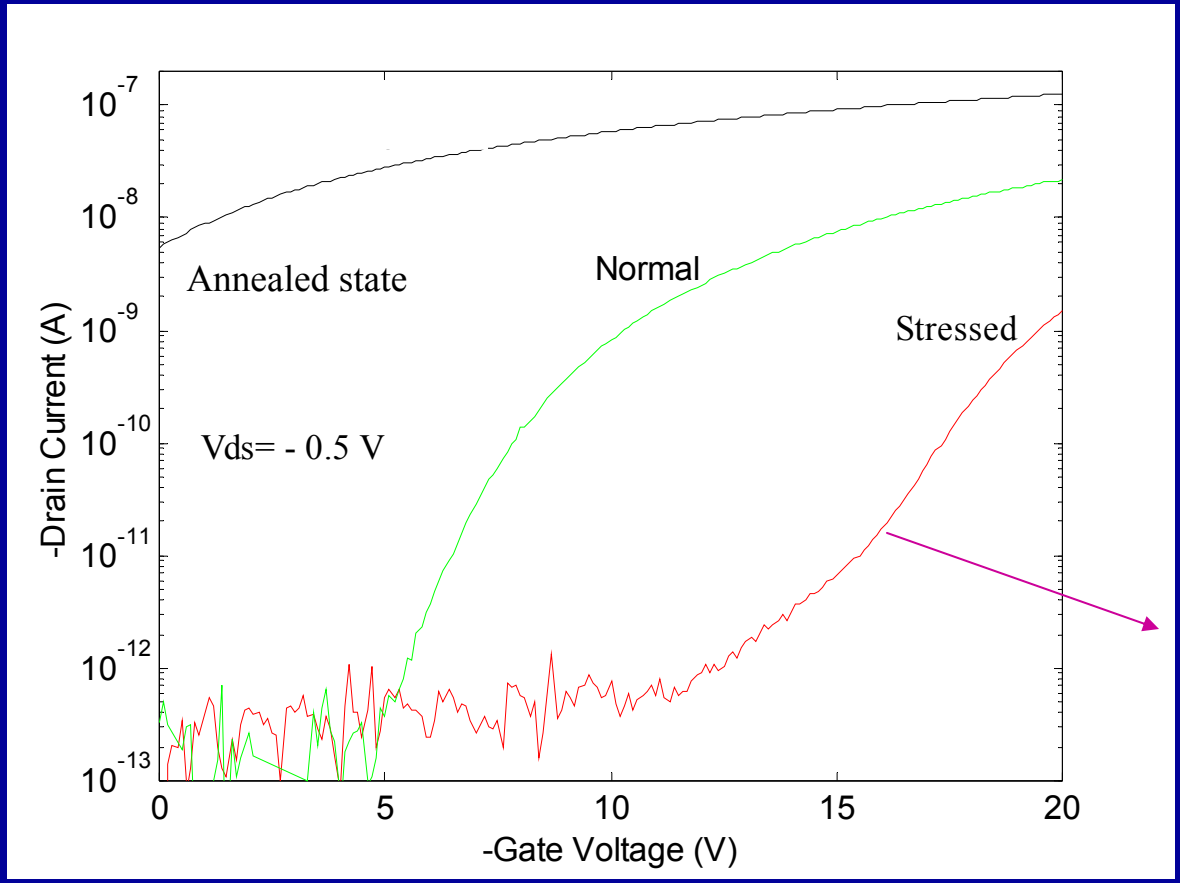
Different traps in different regions of the device.

DLTS Experiments



DLTS spectra of drain-current transients due to gate bias pulse from –20V to 0 V.

Transfer curves for the three different states of a sexithiophene transistor.



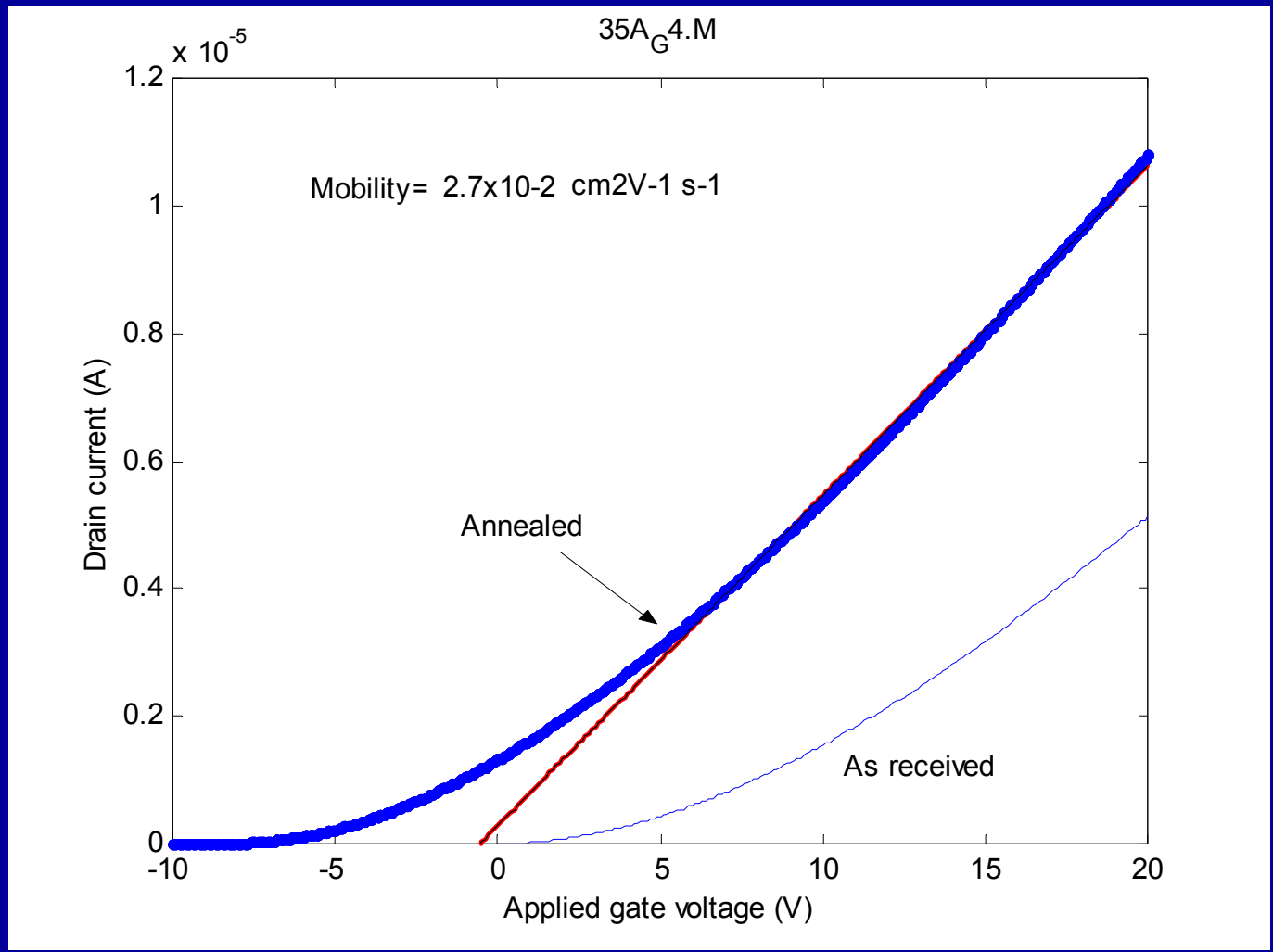
Slope degradation

- The annealed state is obtained by annealing the device up to 340 K under an applied gate voltage of +20 V.
- The stressed state is obtained by applying a negative voltage in the gate over several minutes above 250 K.
- When left resting for some days the device recovers to its normal state. The changes are entirely reversible .

The effect on the device characteristcs

	Annealed state	**Stressed state**
Mobility (cm^2V^{-1} $s^{-1)}$	**$1.1x10^{-3}$**	**$8.9x10^{-5}$**
Threshold voltage (V)	**0.6**	**18.2**

The effect on the device characteristcs



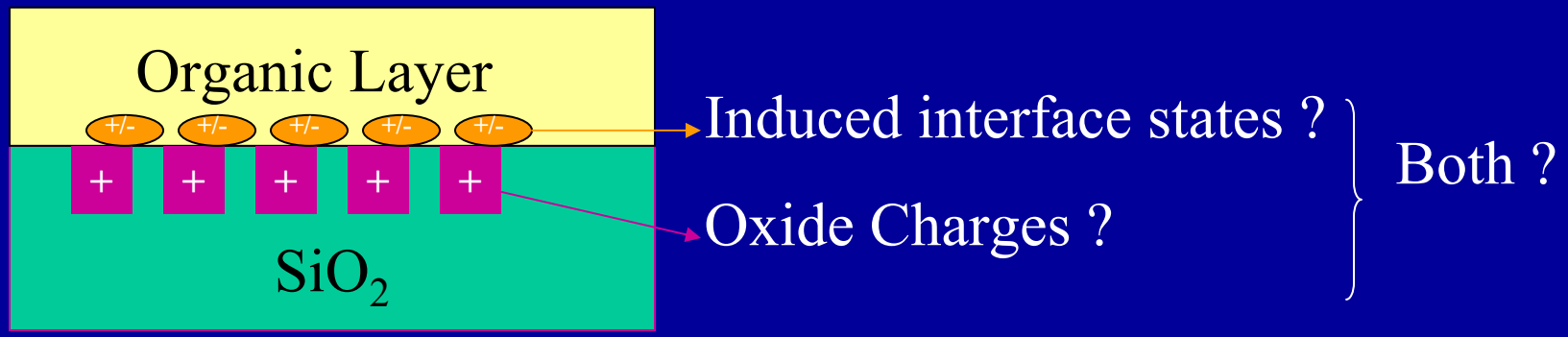
What we know

Negative Vg — Causes degradation.
- Higher threshold voltage.
- Lower mobility.
- Decrease in the drain current.

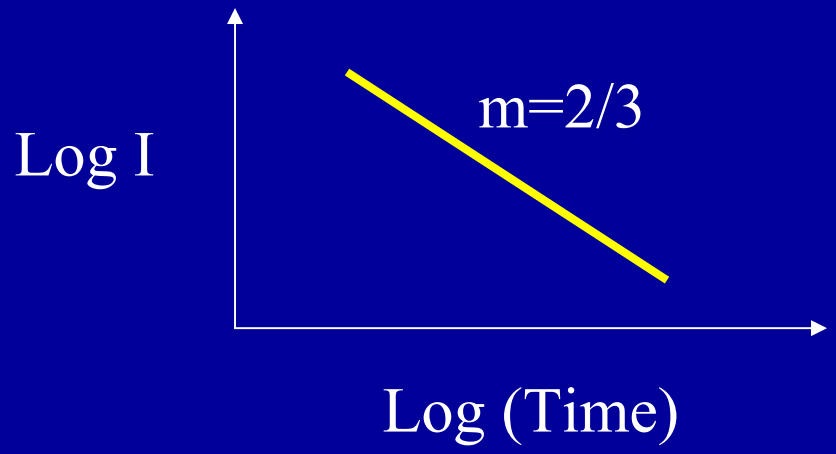
Positive Vg — Tends to restore device degradation.

Annealing under positive Vg
- Induces a high Drain Leakage Current (GIDL current).
- Repairs device degradation caused by the negative gate stress.

Where are located (in the device geometry) the stress induced charges ?



The degradation in conventional n-MOS can be described by a power-law over time, with the exponent usually being in the range of 2/3.



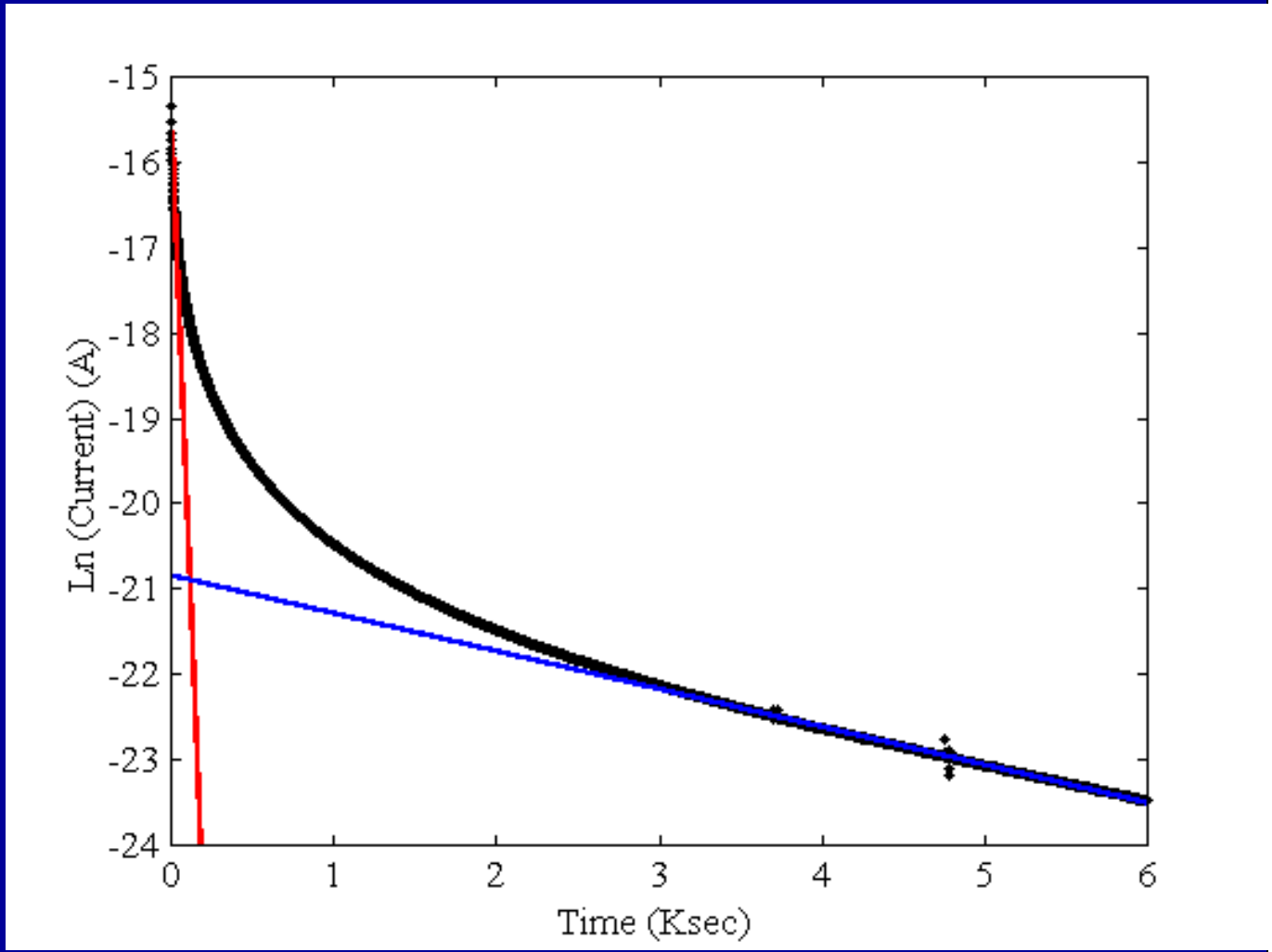
Device relaxation (time constants)

Annealed state

τ_1=20 s

τ_2=40 min.

Normal state



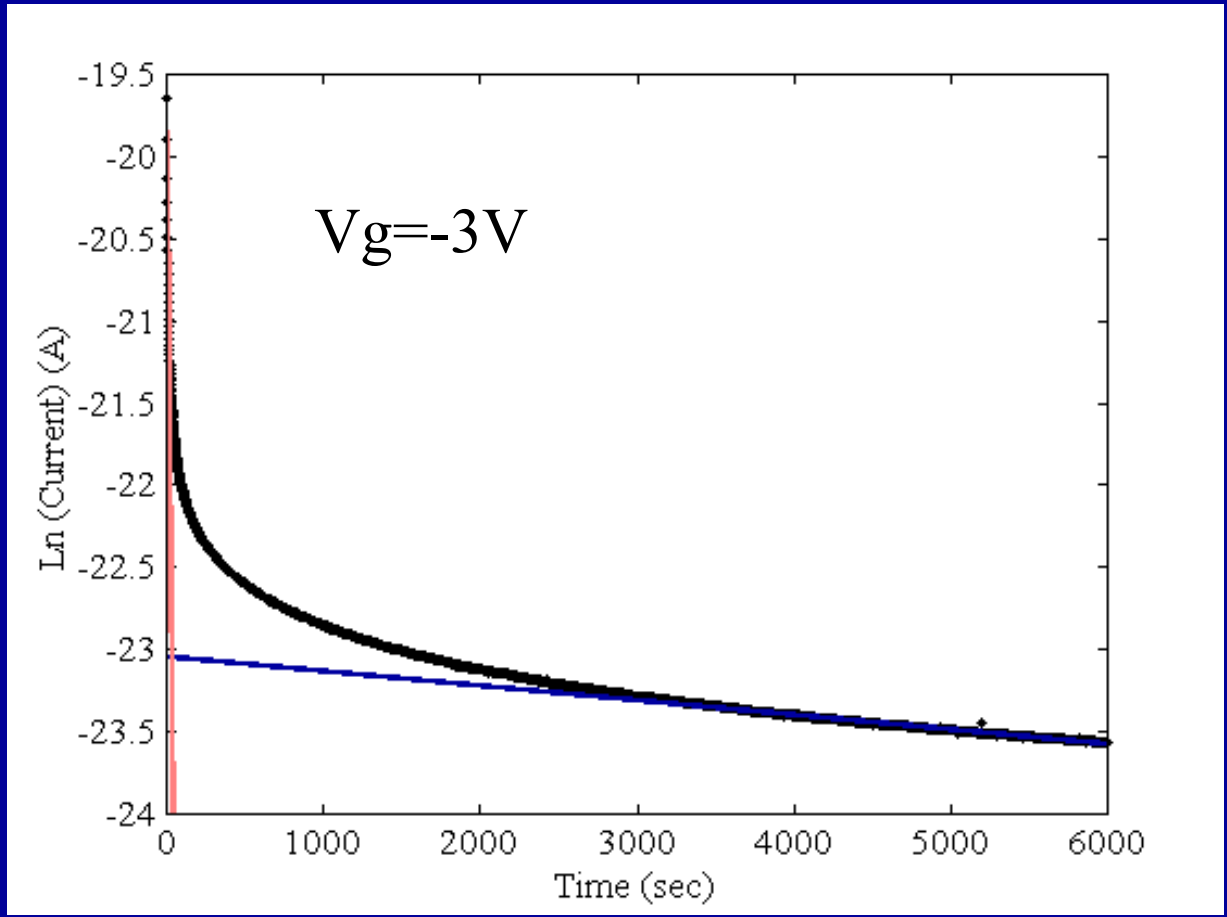
Device relaxation (time constants)

Normal state

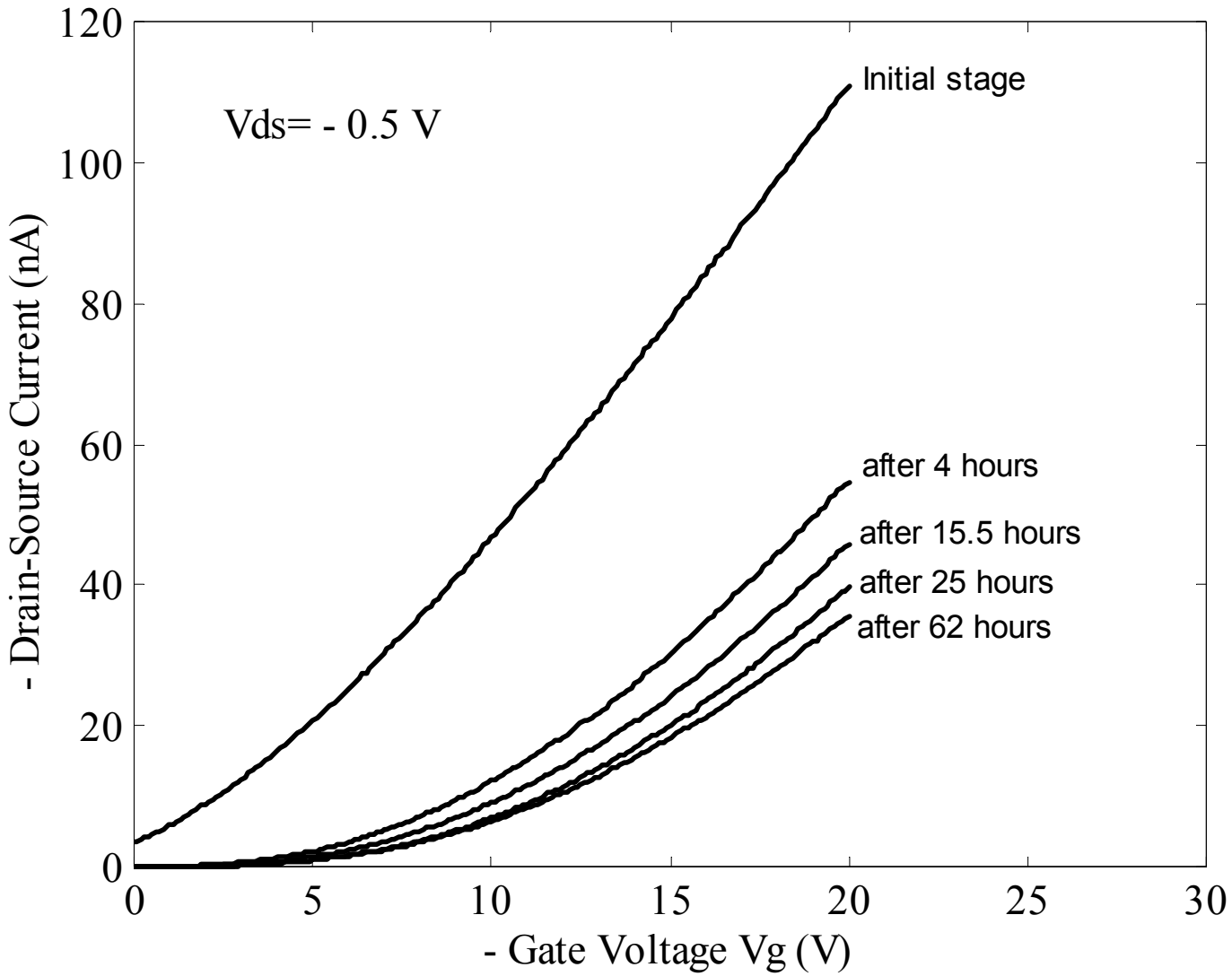
τ_1=10 s

τ_2=2.8 Hours

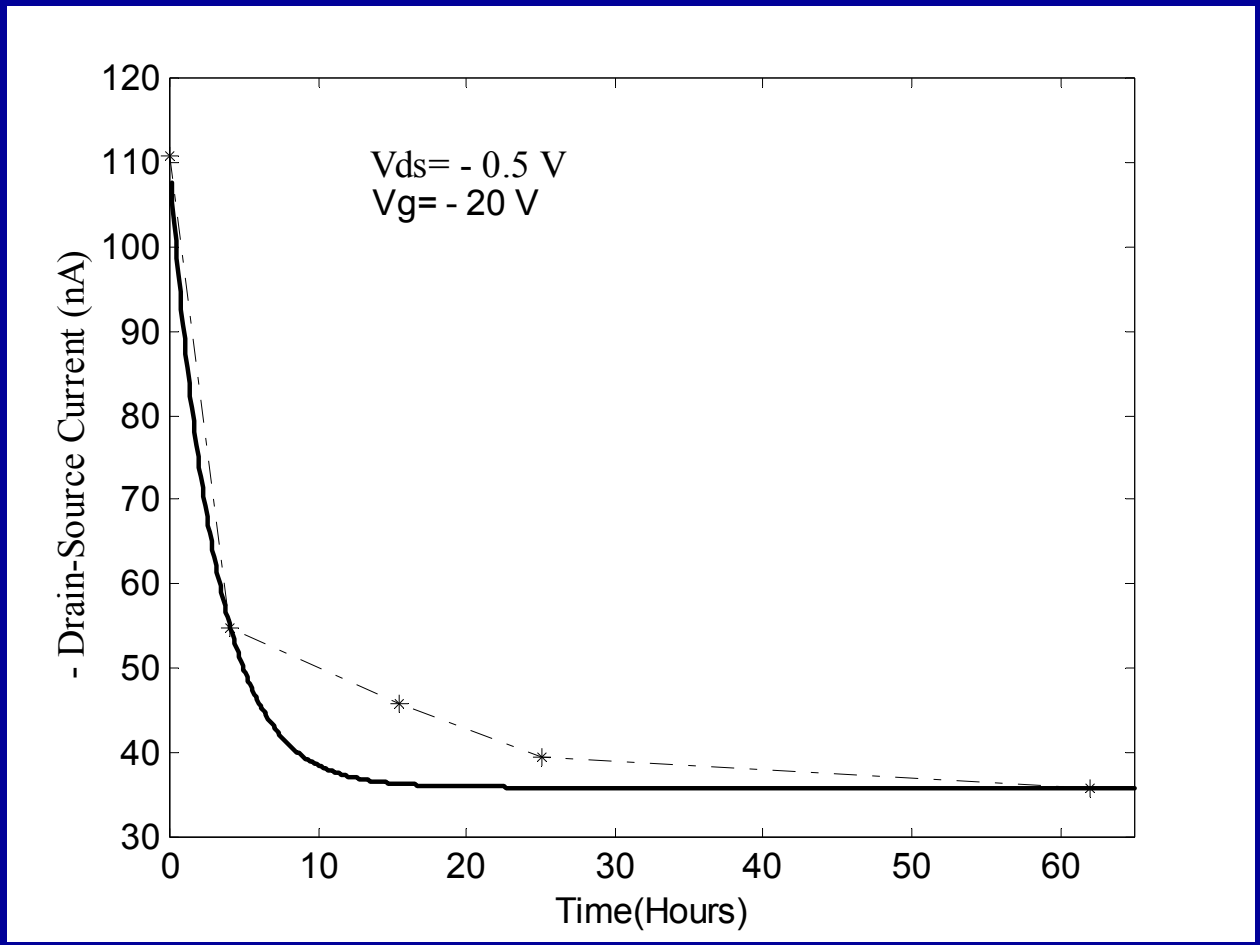
Stressed state



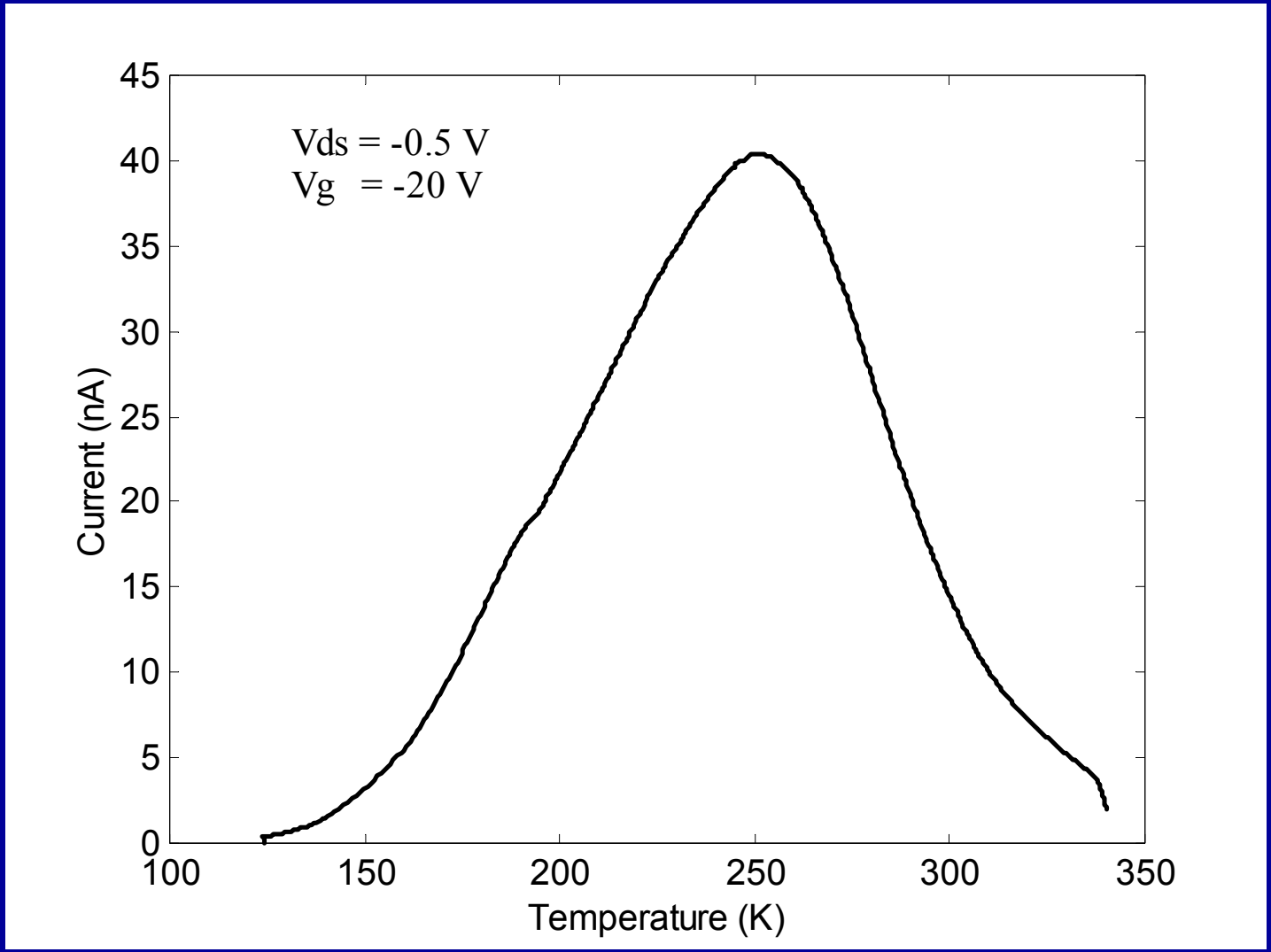
Relaxation from an annealed state to a normal state.



Relaxation from an annealed state to a normal state.



Temperature dependence of the drain current under an applied gate voltage of –20 V



Characterization of stress-induced traps by using a subthreshold current technique

$$S = \ln 10 . \frac{dV_G}{d \ln I_D}$$

$$S = \frac{kT}{q} \ln 10 . \left(1 + \frac{C_A}{C_i} \right)$$

$$S_T = S_O . \frac{1 + (C_A + C_{it}) / C_i}{1 + C_A / C_i}$$

Where:

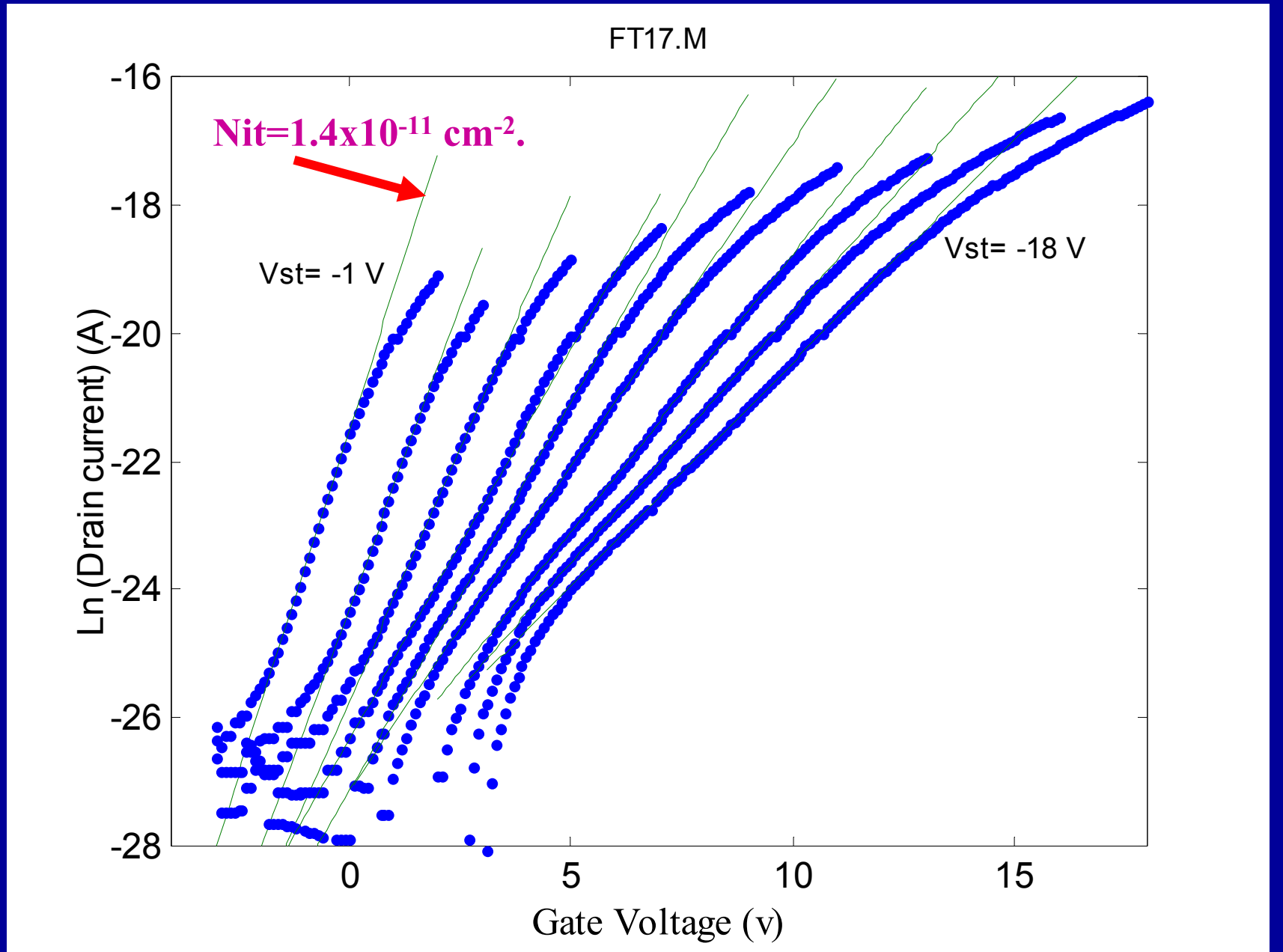
C_A is the capaciatnce of the accumulation layer

Ci is the oxide capacitance

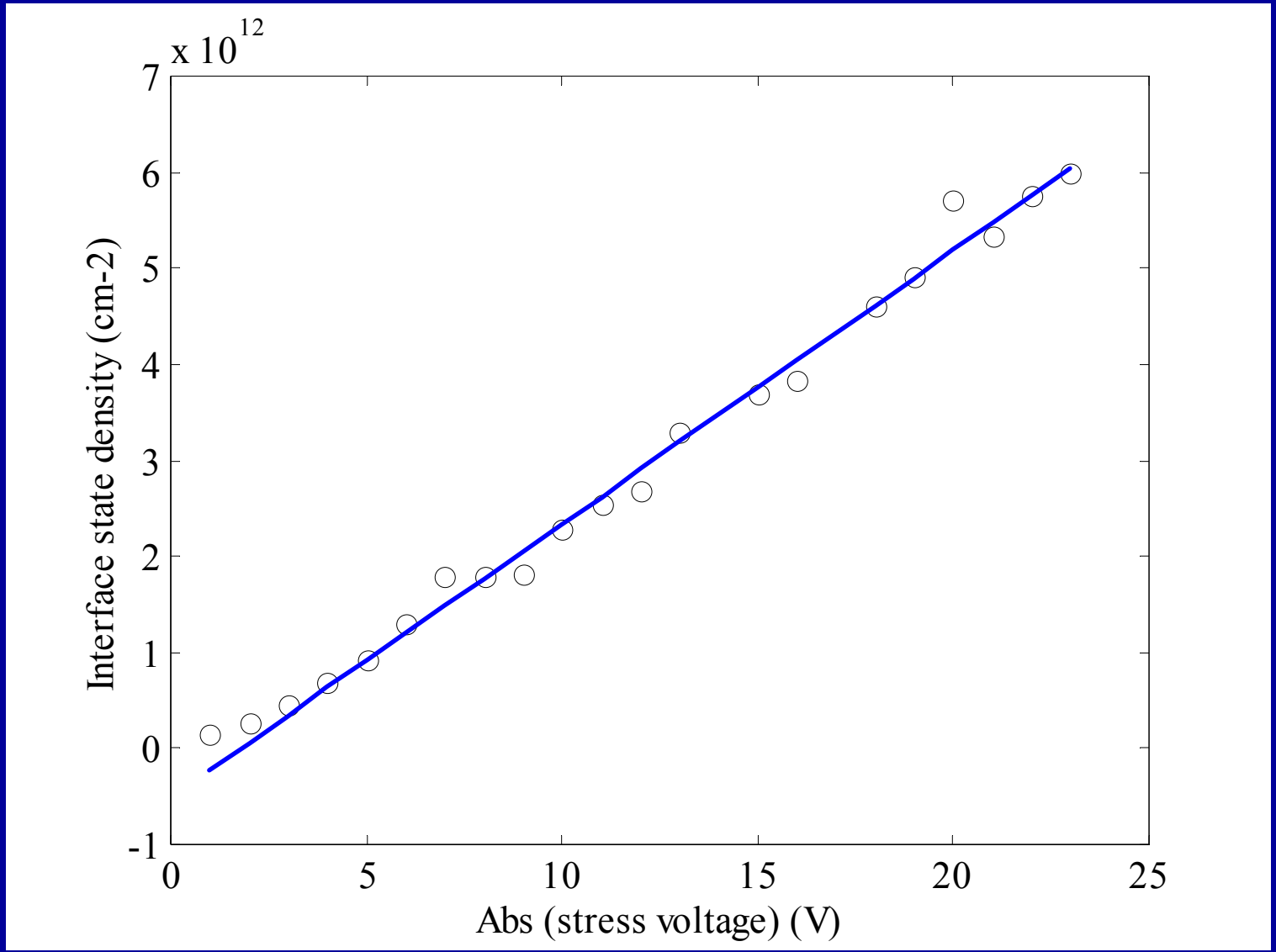
Cit is the capacitance due to interface state density.

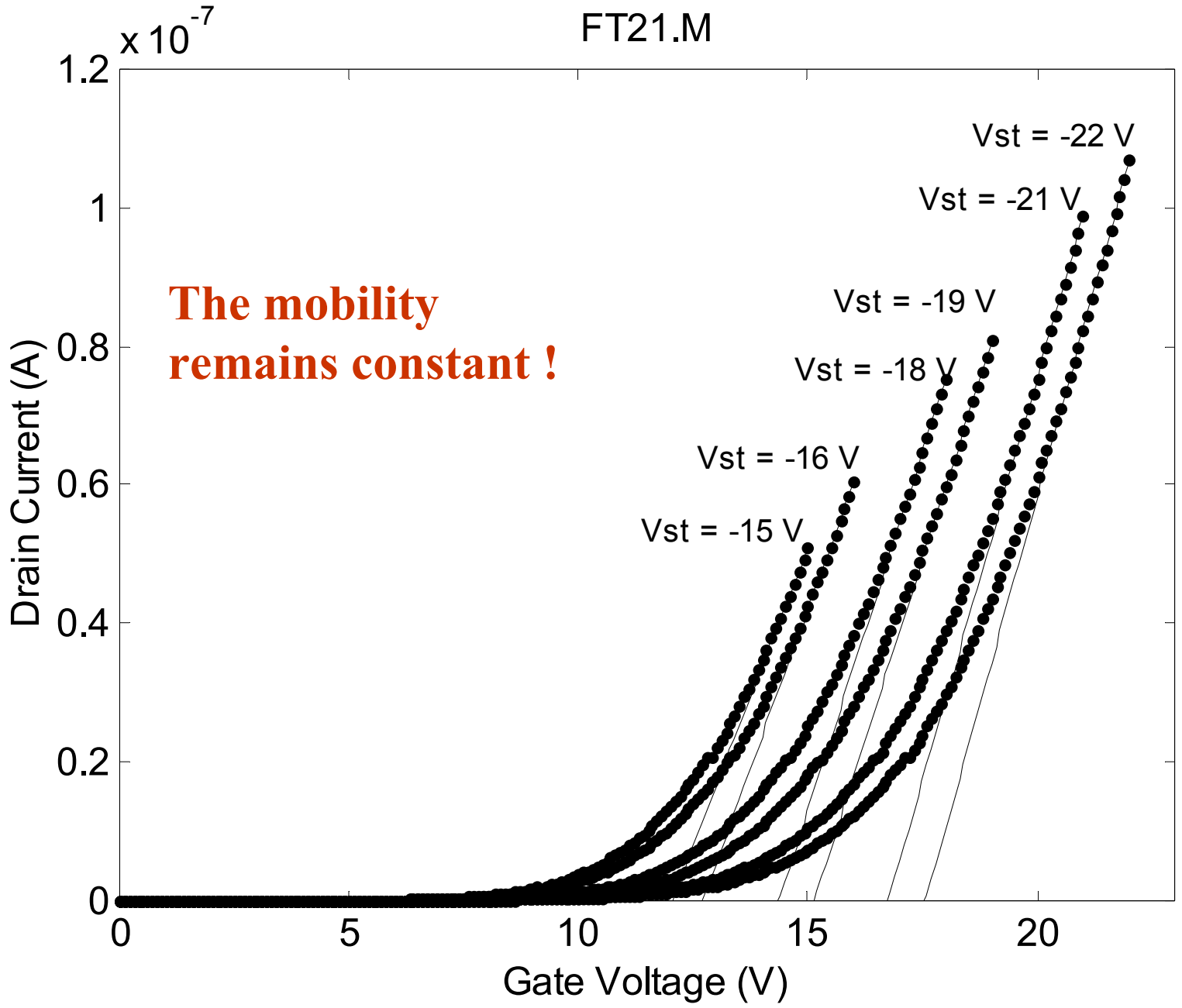
Nit=7x10^{-11} cm^{-2}

J.H. Schön and B. Batlogg (J. Appl. Phys., Vol 89, 336 (2001))


FT17.M
Nit=1.4x10-11 cm-2.
Vst= -1 V
Vst= -18 V
Ln (Drain current) (A)
Gate Voltage (v)
-16
-18
-20
-22
-24
-26
-28
0
5
10
15

Stress induced interface state density




FT21.M
x 10^-7
1.2
1
0.8
0.6
0.4
0.2
0
Drain Current (A)
0
5
10
15
20
Gate Voltage (V)
Vst = -22 V
Vst = -21 V
Vst = -19 V
Vst = -18 V
Vst = -16 V
Vst = -15 V
The mobility
remains constant !

Pseudo-Subthreshold Characteristics

In poly-Si TFT

The exponential dependence of the drian current on the gate voltage is due to the gate induced grain barrier lowering effects, and not due to the accumulation charge density modulated by the gate as the single Si-MOSFET does

Carrier scattering within the grain boundary region can be lumped into the effective mobility model

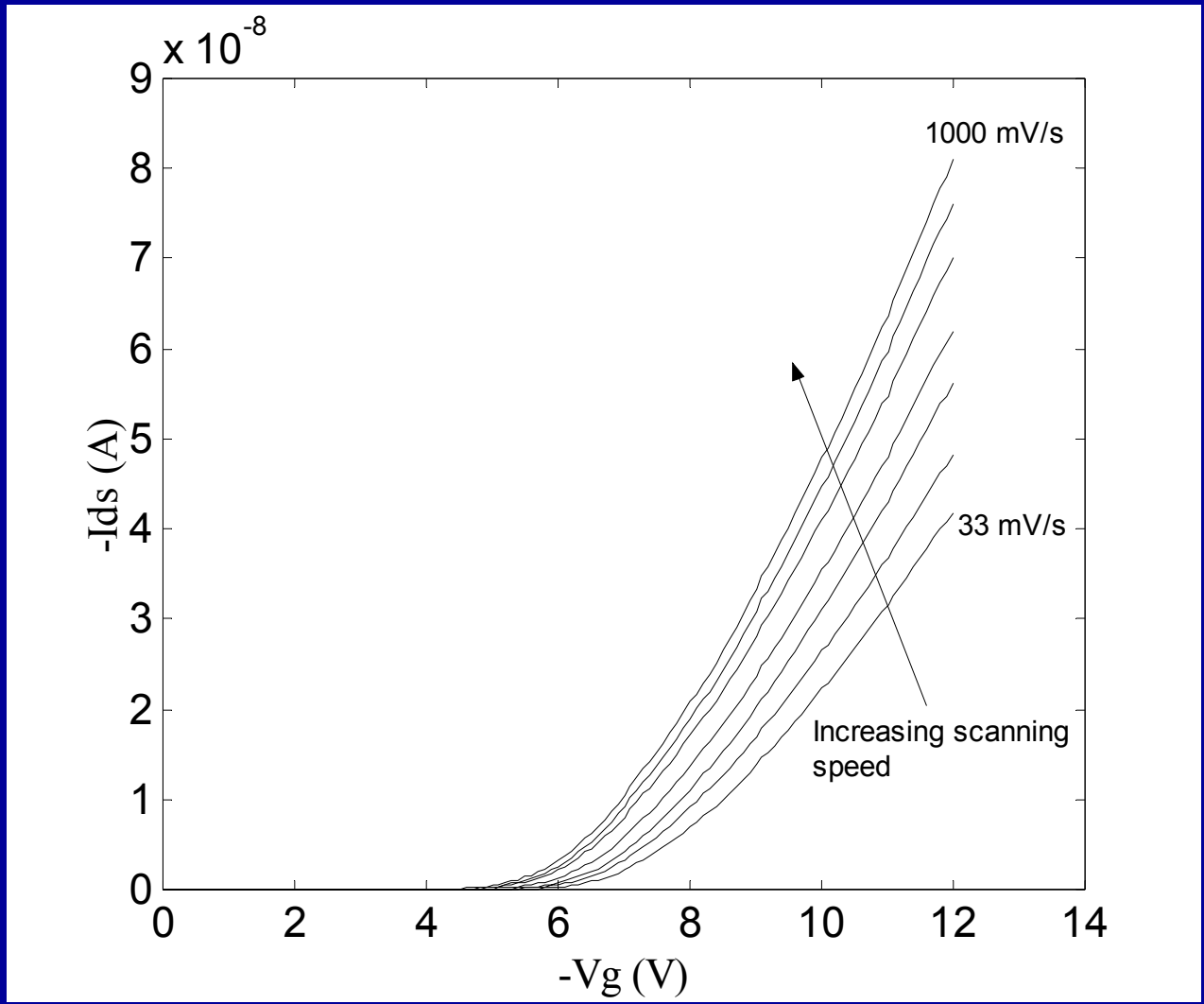
Mechanisms for the GIDL current

- Oxide charges shifts the flat-band voltage and results in an enchanced of the GIDL current.

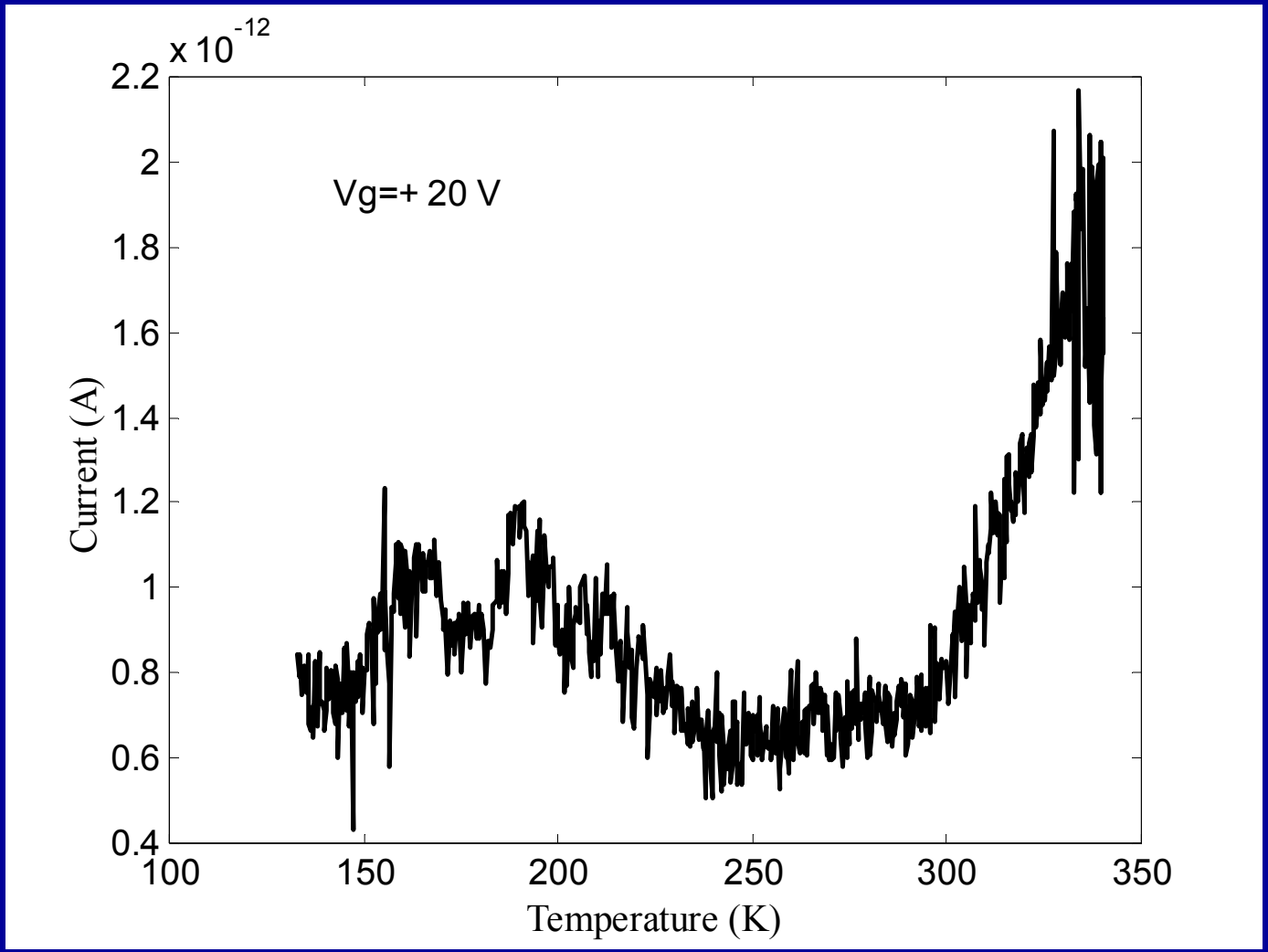
- Generation of interface states may introduce additional band-trap-band leakage mechanisms

Frequency dependent transfer curves

(evidences for fast interface states!)



Thermally Stimulated Currents (TSC)



Conclusions

Degradation is a very complex problem and depends on many (possibly not *a priori* know) technology-sensitive parameters, so further experimental material has to be collected to determine the model parameters.