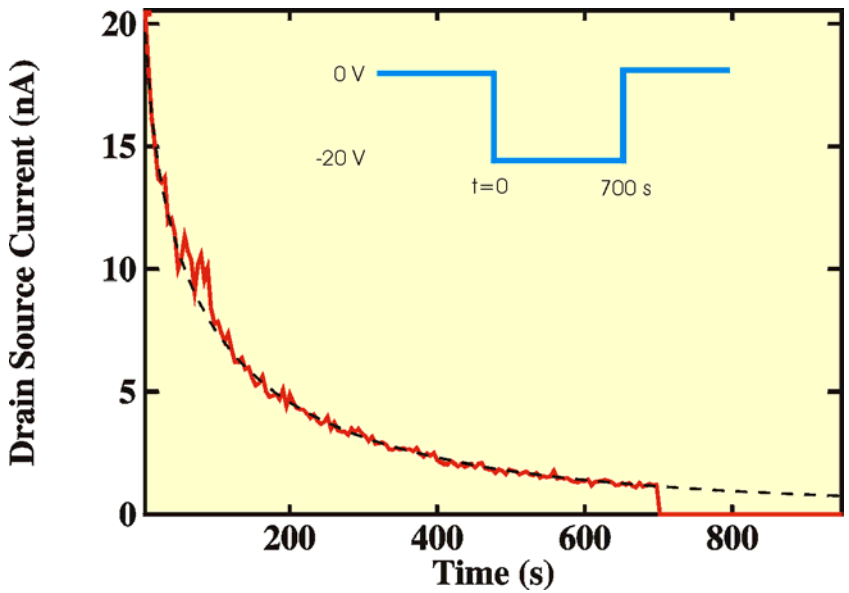
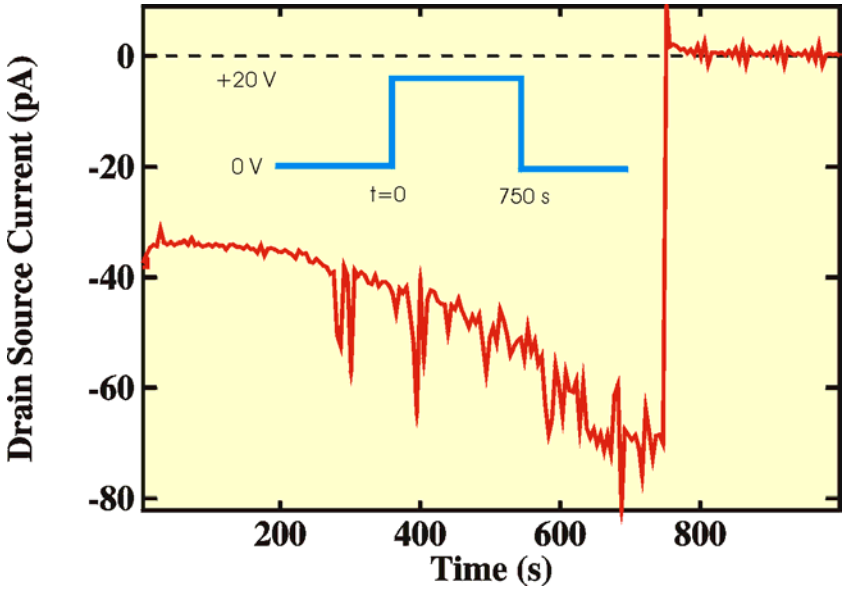
Gate Voltaic Transients



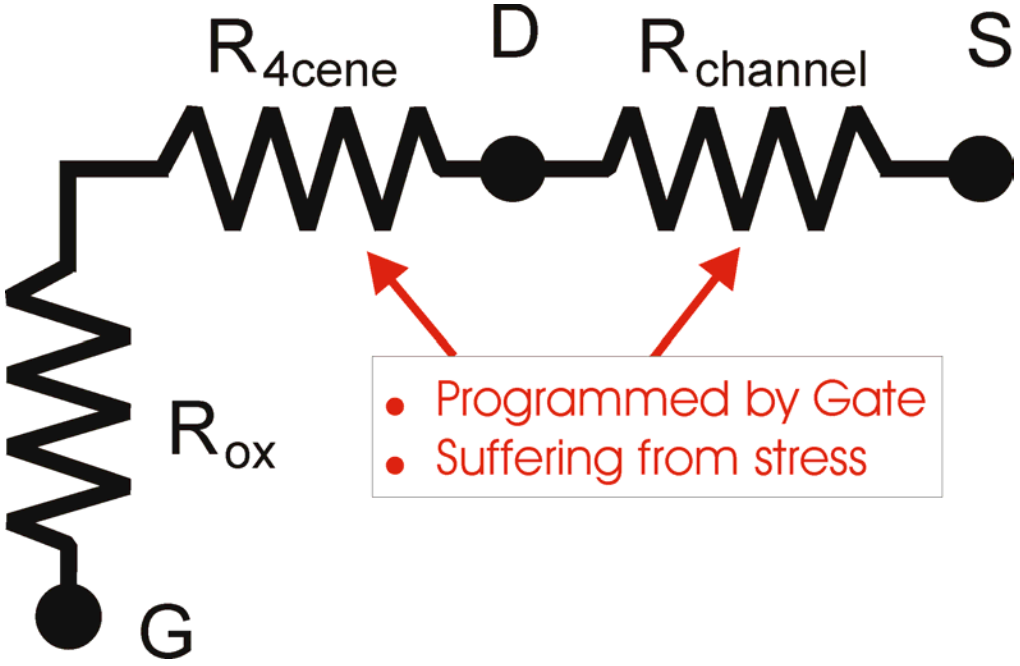


Gate Voltaic Transients

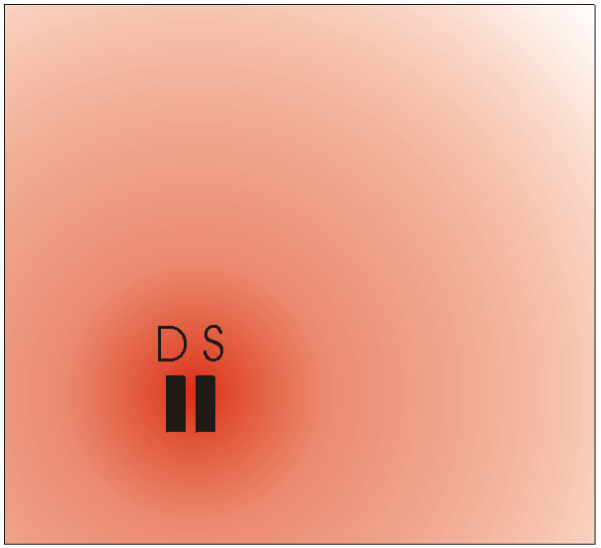
- Not displacement
  - Q = Integrated I is too large ($Q = \mathrm{D}V\,A\,C_{ox}$, $C_{ox} = \varepsilon_0\varepsilon_r/d_{ox}$ $Q = 6.91\mathrm{x}10^{-7}$ C)
  - When switching off the voltage, Q doesn't come out.
  - For positive V_G: not same (magnitude of) current.
- Follows exponent of square-root-of-time behavior:

$$I_{ds} = I_0 \exp(-(t/\mathrm{t})^{0.5}) + I_{\mathrm{off}}$$

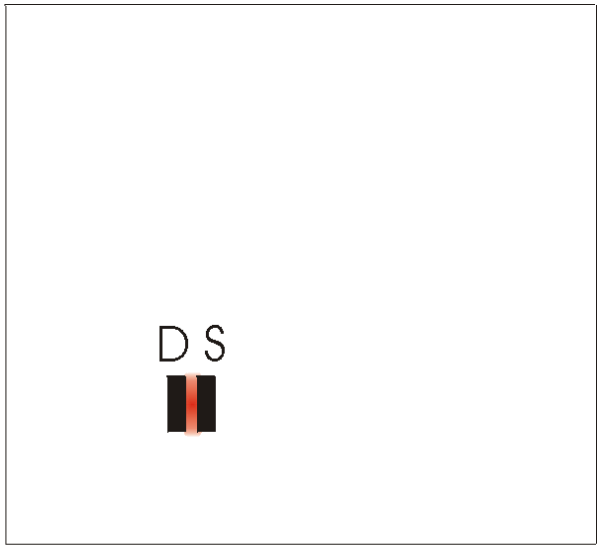
The Model


R4cene
D
Rchannel
S
Rox
G
Programmed by Gate
Suffering from stress

The Model



Leakage Current

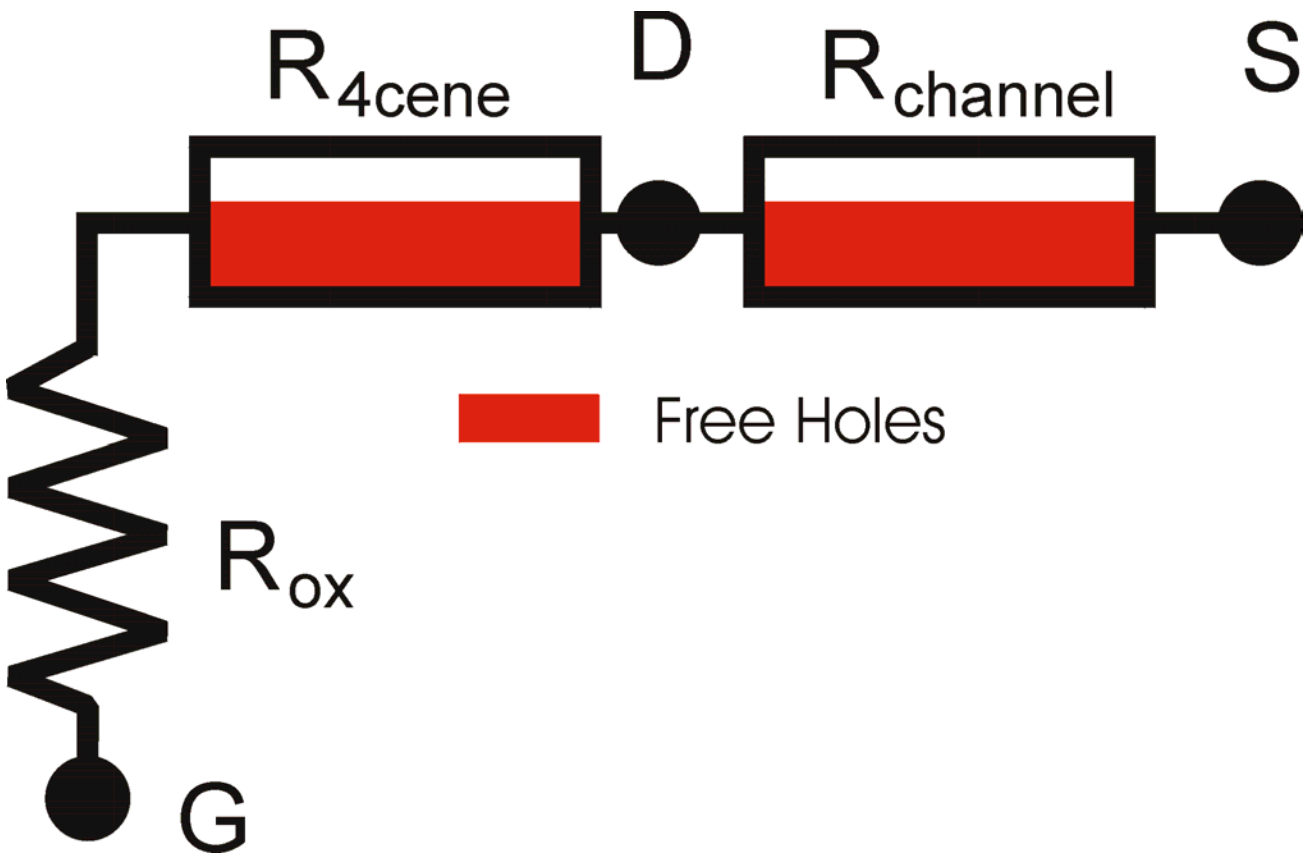


Channel Current

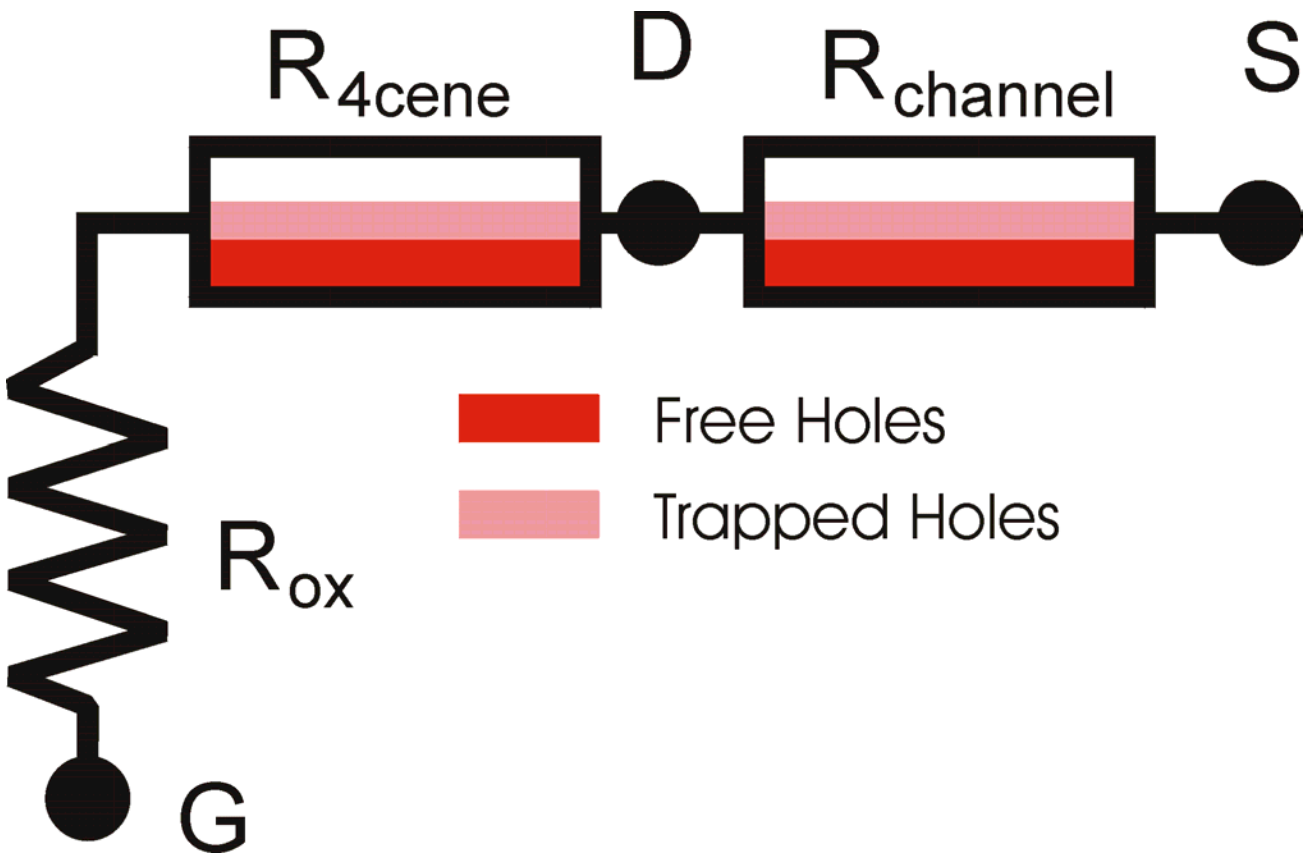
Leakage current and channel current about the same magnitude

Both suffer from trapping of free carriers which increases the resistivity.

The Model: Transient Behavior

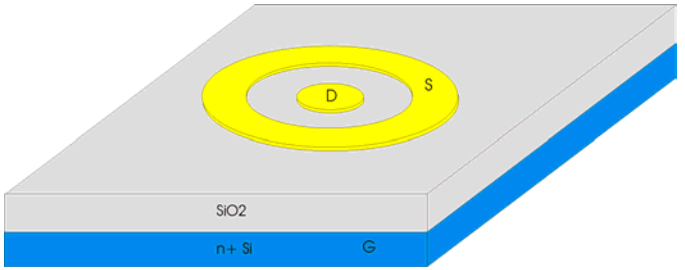


The Model: Transient Behavior



The Solution

Circular FETs



Poor man's alternatives:

- Scratching/isolating single devices
- Also connect pads on side of device to source
- Measuring always with $\mathrm{Vg} = \mathrm{Vd}$

Note: there is no use in masking the edges!

Ideas / Comments

To set up the **ultra-fast pulse** experiment (Lecroy-Agilent): IEEE cables (2) and interface card (1) are needed urgently.

To study the interfaces of FETs, **sandwich structures** are needed

The FlexiFET program

How to increase the luminescence

Use **half-locus** curves

$$Vg = (Vd+Vs)/2$$

In this way, the drain-source voltage can be increased, without ultrapassing the oxide breakdown voltage anywhere.

Example