

Electronic Complements

Second call exam

28 January 2013, 9-12

(Duration: 3 hours)



UNIVERSIDADE DO ALGARVE



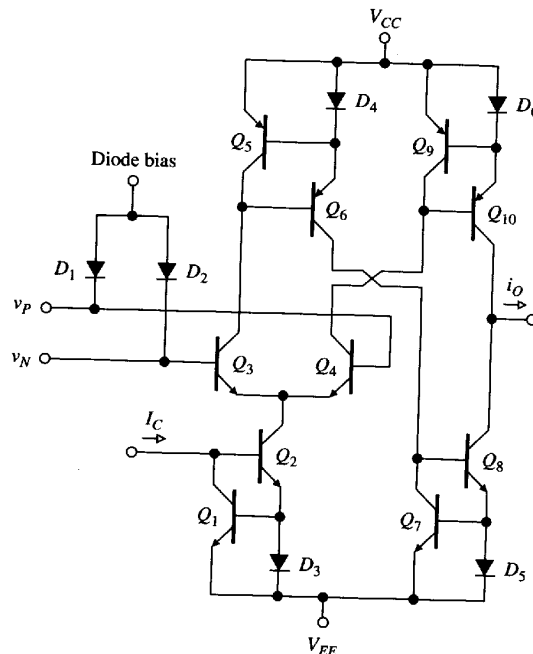
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- Write your name, student number and course on all sheets you hand in.
- Talking is not allowed. If you do it, your exam will be canceled. Switch off your cellular telephone.
- If you give up, write "I Desist" on the exam sheet and hand it in.
- The exam has 4 questions and the maximum score for each is written in brackets.
- Write legible.
- Good luck!

Question 1 (5)

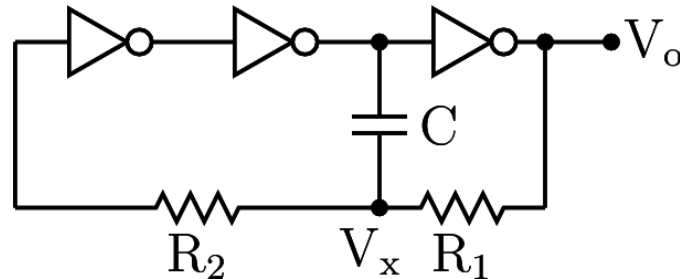
The figure below shows an operational transconductance amplifier (OTA). The heart is formed by the diodes D_1 , D_2 and the transistors Q_3 and Q_4 , while the rest of the transistors and diodes are four Wilson current sources/mirrors: Q_5 - D_4 - Q_6 , Q_9 - D_6 - Q_{10} , Q_1 - D_3 - Q_2 , Q_7 - D_5 - Q_8 . Assume all $\beta = \infty$.

The current I_C comes from a voltage-controlled current source, $I_C = aV_x$, and to i_o a load resistance R_L is connected, V_y is defined as $V_p - V_n$.



- What is the collector current of transistor Q_2 ?
- How many quadrants does this analog multiplier have?
- How to make a voltage-controlled current source, $I_C = aV_x$?
- Show that the output is proportional to V_x and V_y .

The figure below shows a logic oscillator made of three logic inverters. Note that the input voltage of these inverters is 'clamped'. This means that they cannot exceed 0 and V_{DD} . In case this occurs, they are fixed at these values (as if the inputs were then ideal voltage sources)



- ### Question 3 (5)

The circuit diagram shows a Class AB push-pull output stage. At the top, a V_{CC} supply is connected to a network of resistors $R1$ and diodes $Q5$ and $Q6$. This network is connected to the bases of transistors $Q3$ and $Q4$, which form a V_{BE} multiplier. The emitters of $Q3$ and $Q4$ are connected to the bases of the output transistors $Q1$ and $Q2$. The emitters of $Q1$ and $Q2$ are connected to ground through resistors $R2$. The output voltage V_{out} is taken from the collector of $Q2$. The input voltage V_{in} is applied to the base of $Q1$. A capacitor C is connected between the emitters of $Q1$ and $Q2$. Two current sources I_B are connected to the bases of $Q1$ and $Q2$. The current I_1 is indicated flowing into the base of $Q1$ and out of the base of $Q2$.

- ### Question 4 (5)

An FM signal is being modulated over the range of $1 \text{ MHz} \pm 10 \text{ kHz}$, with a modulation frequency of 1 kHz . Using a 4046A PLL, design a circuit to demodulate such a signal. The central frequency of the VCO is given by

$$f_0 = \frac{k_1}{R_1 C} v_E + \frac{k_2}{R_2 C}$$

with v_E defined relative to $V_{DD}/2$, and k_1 and k_2 depending on the PLL (see datasheet). Show the signals at various relevant points of the circuit

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Complementos de Electrónica
Exame época recurso
28 de Janeiro de 2013, 9-12
(Duração: 3 horas)



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- Escreva o seu nome, nº de aluno e curso em todas as folhas que entregar.
 - Não é permitido falar com os colegas durante o exame. Se o fizer, terá a prova anulada. Desligue o telemóvel.
 - Caso opte por desistir, escreva “Desisto”, assine e entregue a prova.
 - O exame tem 5 perguntas e a cotação de cada aparece entre parêntesis.
 - Faça letra legível.
 - Boa sorte!
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Pergunta 1 (4)

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